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ELECTRONIC SUPPORTING UNITS FOR SOUNDING ROCKET PAYLOADS,(U)
MAR 78 R W CHARRON, T J CAMPBELL, T DIMILLA F19628-76-C-0211
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(6) ELECTRONIC SUPPORTING UNITS FOR SOUNDING ROCKET PAYLOADS

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(14) SCIENTIFIC-

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(16) 7670 (17) 06

(15) F19628-76-C-0211

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Scientific Report No. 2

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFGL-TR-78-0163	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) ELECTRONIC SUPPORTING UNITS FOR SOUNDING ROCKET PAYLOADS		5. TYPE OF REPORT & PERIOD COVERED Scientific - Interim 6. PERFORMING ORG. REPORT NUMBER Scientific Report No. 2
7. AUTHOR(s) Robert W. Charron Lawrence P. Smart Thomas J. Campbell Thomas DiMilla, Jr.		8. CONTRACT OR GRANT NUMBER(s) F19628-76-C-0211
9. PERFORMING ORGANIZATION NAME AND ADDRESS Wentworth Institute of Technology 550 Huntington Avenue Boston, Massachusetts 02115		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62101F 76700607
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Geophysics Laboratory Hanscom AFB, Massachusetts 01731 Manager/Joseph F. Geary, Jr., LCR		12. REPORT DATE 31 March 1978 13. NUMBER OF PAGES 81
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release: distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Digital Timer
SPICE Sensor Deployment System
Logic Control Unit
Programmable Data Collection Point Spacing
Inexpensive Sounding Rocket Flight recorder
Compression Amplifier
Vibration and Shock Calibration Data

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Six-Switch Digital Timer

Section one of this report covers the development of a six-switch digital timer suitable for use by sounding rocket payloads. Its features include six SPDT relay switch outputs, a maximum time-out in excess of 4½ hours, and simple, effective programming using a minimum of peripheral equipment.

SPICE Sensor Deployment

Report section two contains an explanation of the modifications

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

19. Key Words

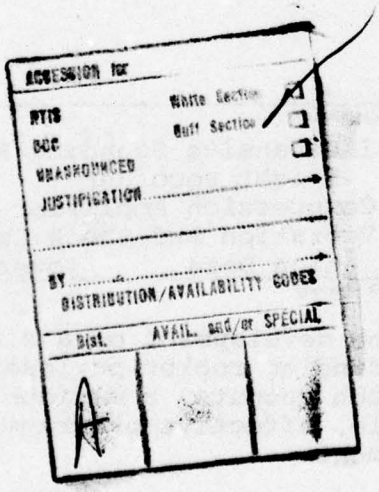
Capacitor Discharge Firing Unit
Function Monitor
Flight Data

20. Abstract

Spice Sensor Deployment (cont.)
that were needed by the Hi Star Sensor Deployment System to adapt it for SPICE and ZIP program use. These modifications accommodated an increase in sensor size and mass, and provided an offset between the stepping inward/outward modes of operation. Programming facilities were also added enabling one to adjust Data Collection Point positions and mode offset spacing.

Rocket-Borne Vibration Recorder (ROVIR)
This section of the report provides a description of an unsuccessful attempt to modify an inexpensive tape cassette drive system for use as an in-flight recorder by sounding rocket payloads. More successful was the portion of the task that required developing a special compression amplifier that acted as an interface between piezoelectric vibration sensors and an FM/FM Telemetry system.

C.D.S.F.U. Function Monitor Update
New data has become available that illustrates the second method of C.D.S.F.U. function monitoring. This method, employing a voltage divider, monitors the voltage level of the capacitor bank when it is discharged, igniting EEDs.



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FOREWORD

This report, divided into four sections, relates the results of work at Wentworth Institute of Technology's Air Force Contracts Department as performed under the sponsorship of the Air Force Geophysics Laboratory through Contract AF19628-76-C-0211.

The items reported on -- a digital timer, an IR sensor deployment system, a vibration sensing system and the second function monitor of an EED firing system -- are but a few of the devices designed and fabricated to support scientists who use sounding rockets and satellites as research tools. Sometimes the devices are new in concept, but more often they are modifications of previous designs, such as the IR sensor deployment system.

The original design concept for the IR sensor deployment system was generated in early 1969 fulfilling the requirements of Project #AT3.726. Since then, it has been successfully used in 11 more sounding rocket flights. Each time, the design was upgraded to meet ever more stringent project specifications. This practice of expanding a design to fit the task, improves reliability and reduces development costs.

Six-Switch Digital Timer

1.0 INTRODUCTION

The ZIP, SPICE and IRBS projects' programming requirements could not be satisfied by using presently available timers. A new design was required.

2.0 DESIGN OBJECTIVES

2.1 Environment

Power:	28 4 VDC
Temperature:	-40 F to _140 F
Vibration:	0.15 g /Hz 100 - 1,000 Hz w/6 DB/oct roll off at 20 Hz and 2,000 Hz
Shock:	50 G's, 11 msec. half sine wave

2.2 Programming

The unit must be easily programmed in the field, using a minimum of peripheral equipment.

2.3 Output

The output should consist of six independently programmed SPDT switches capable of handling moderate amounts of current (approximately 1 Amp).

2.4 Master/Slave Operation

It would be desirable to be able to extend the number of outputs beyond six by operating a second unit as the slave to the first: doing so would ensure the synchronization of all twelve outputs.

2.5 Inhibit Capability

Another design objective is to provide some means of inhibiting the functioning of any one output when the

occasion demands. A redundant output could be inhibited by the output of the first one to function.

2.6 Timing

Range - A minimum total range of fifteen minutes is satisfactory.

Accuracy - In general a ±1% over the specified voltage and temperature range is acceptable.

2.7 Control/Monitoring

Provisions must be made to control and monitor the unit's operation remotely during operational checks of the payload as well as in the launch configuration.

2.8 Results

Several design concepts were considered. Three of them were explored extensively through to the completed breadboard stage. The design approach selected was a spin-off of an earlier design used successfully by the Hi-Star and Hi-Hi-Star projects. It was expanded and modified by switching from TTL to CMOS Electronics. Its features and specifications are as described in the balance of this report section.

3.0 PHYSICAL DESCRIPTION (Figures 1a, 1b)

3.1 Dimensions

Height:	1 7/8"
Width:	4 7/8"
Length:	5 5/8"
Mounting:	Provisions for mounting consist of four slots for #10 screws located at the corners of a 3 7/8" x 5 3/8" rectangular layout.

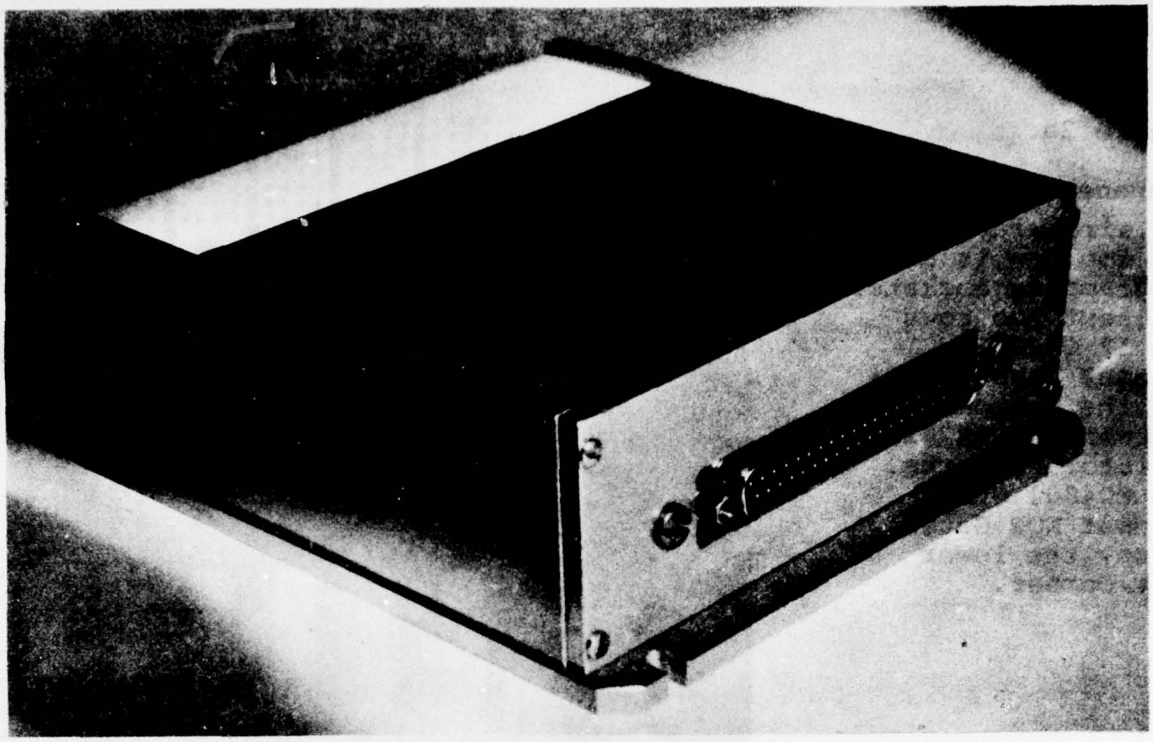


Figure 1a. Front view of Digital Timer Model WI 206

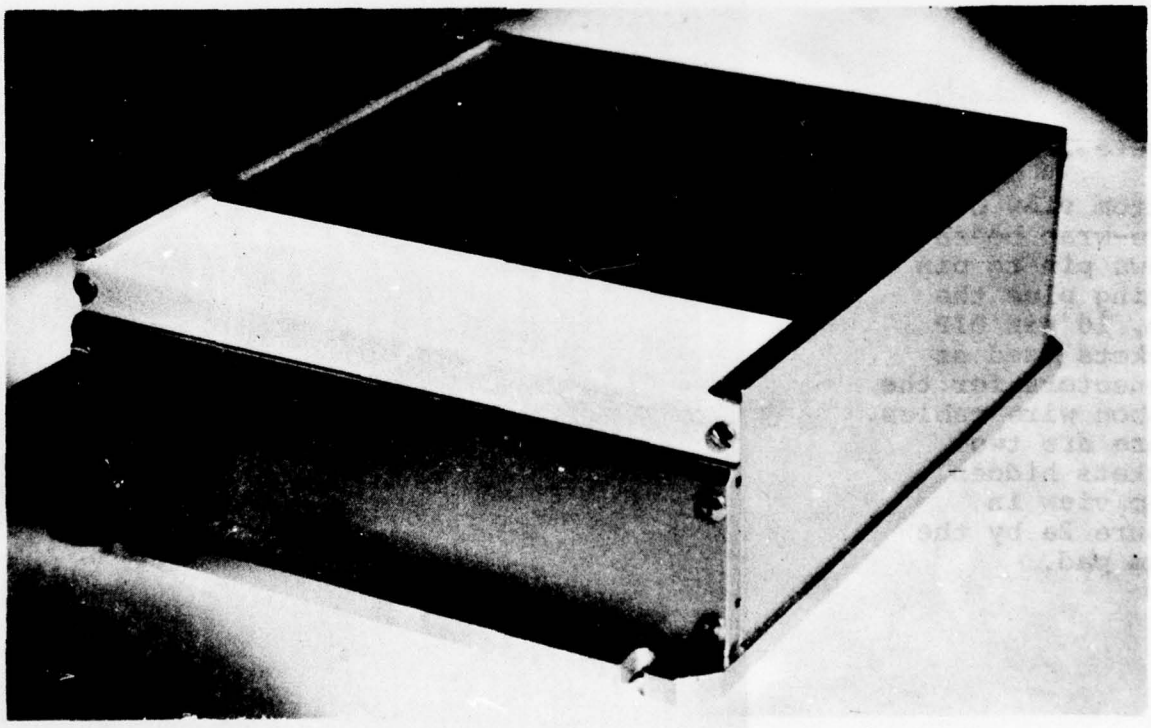


Figure 1b. Rear view showing removable plate that covers programming facility

Figure 2a.

Component side of the wire-wrap board. The top row is six programming sockets; the next two rows are 12 CD4068 8 input NAND gates; and the bottom row contains 6 CTS7625 resistor networks. Two CD4001 Quad 2-Input NOR Gates occupy the lower left corner.

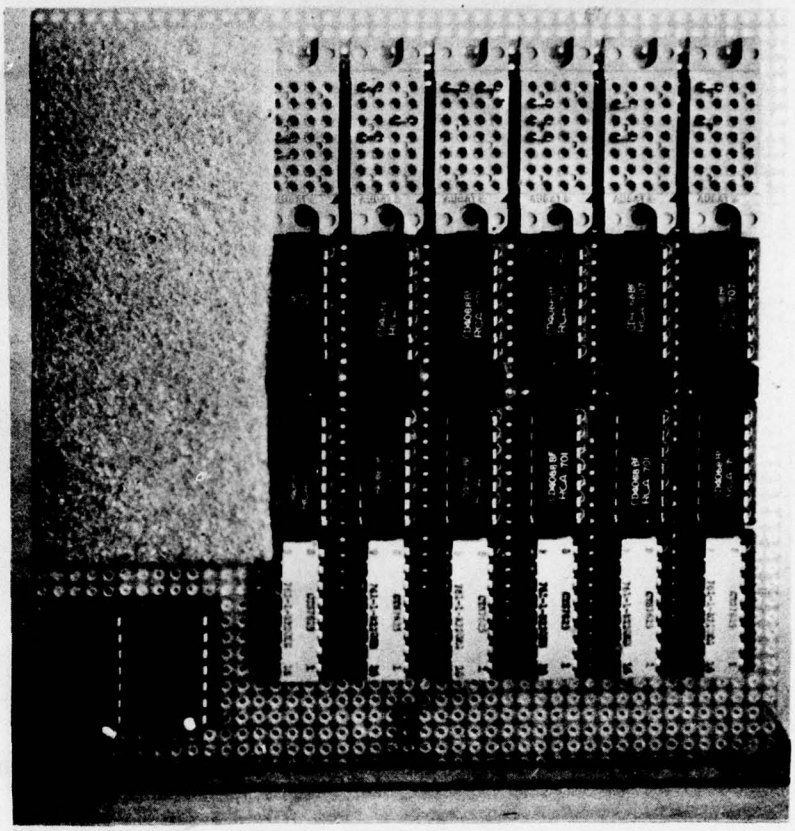
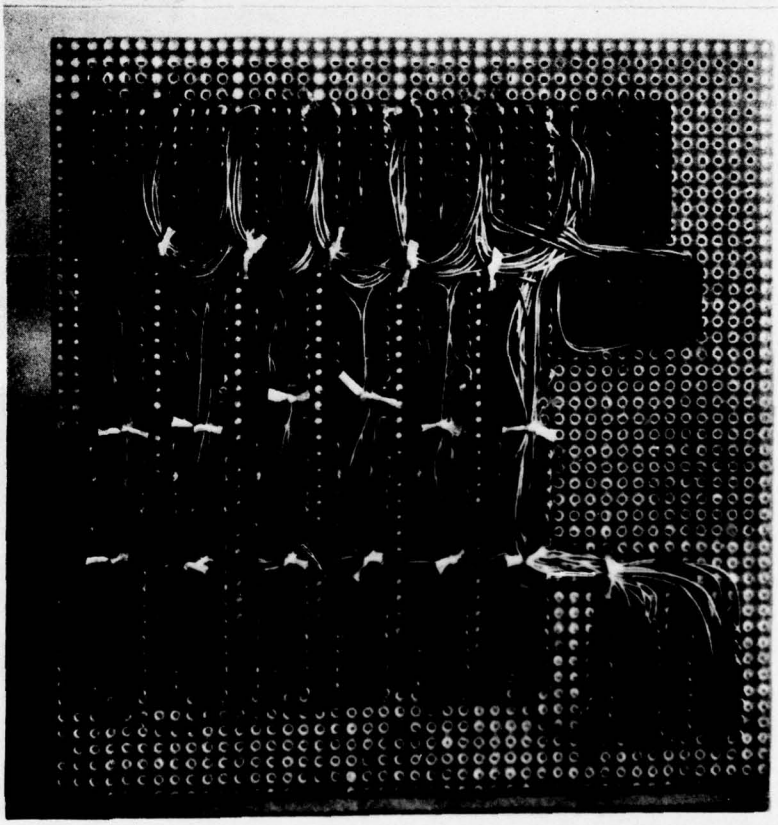


Figure 2b.

Bottom view of wire-wrap board shows pin to pin wiring plus the two, 16 pin DIP sockets used as connectors for the ribbon wire cables. There are two sockets hidden from view in Figure 2a by the foam pad.



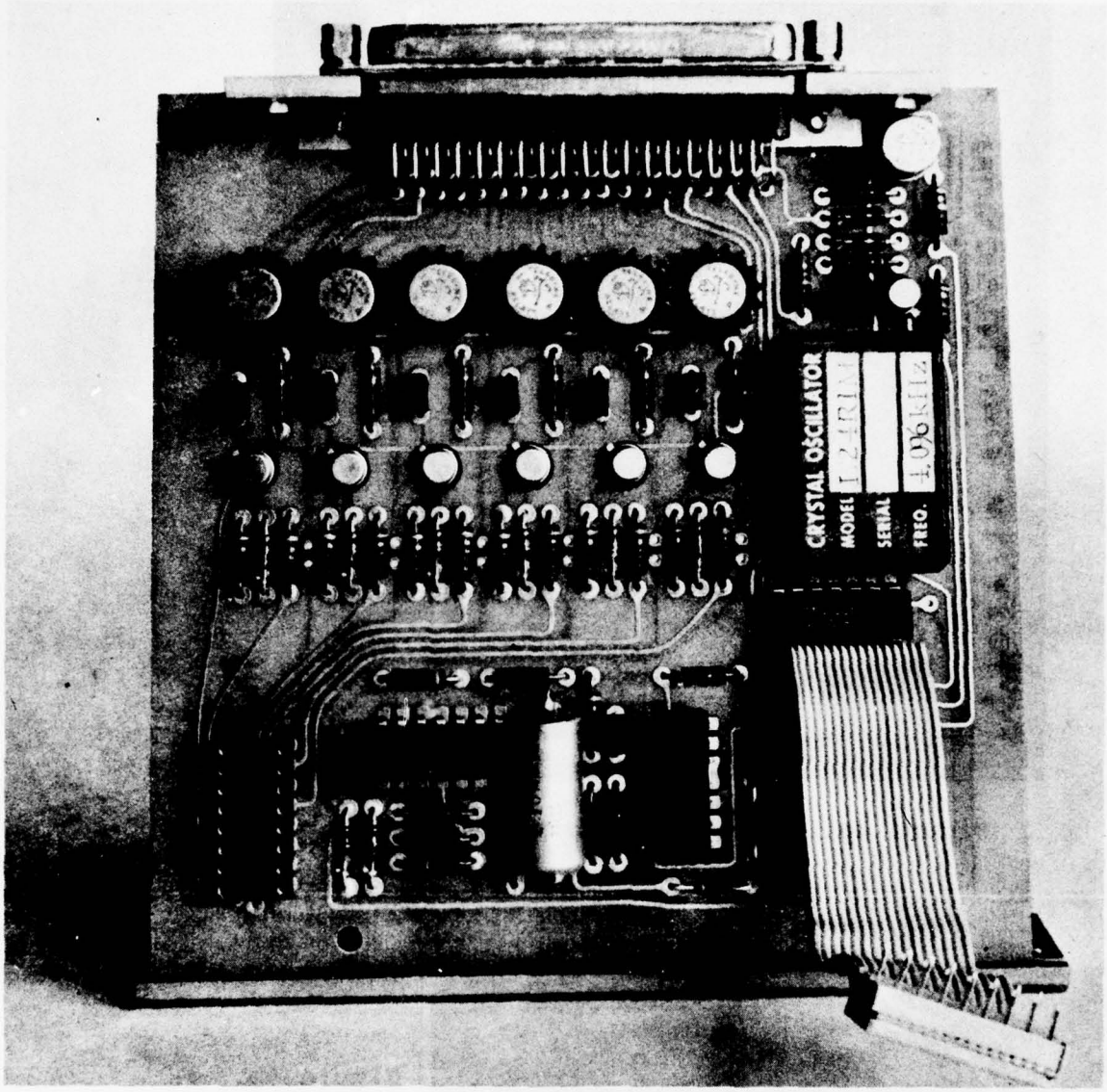


Figure 3. Component side of the p.c. board. Note ribbon wire cable used to electrically connect the p.c. board to the wire-wrap board.

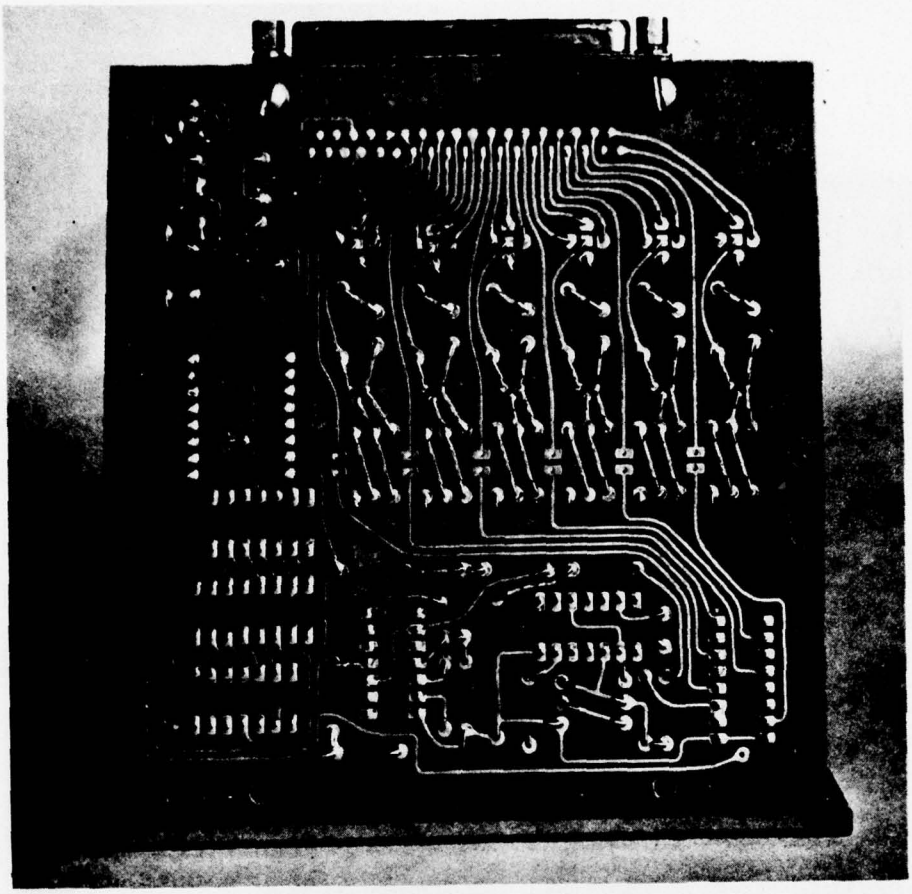


Figure 4a. Bottom of the p.c. board

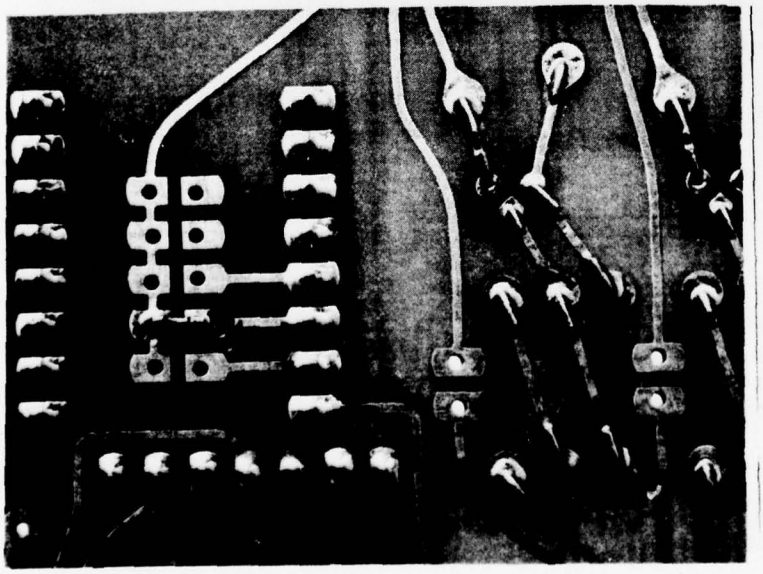


Figure 4b.

Enlarged section shows p.c. pattern used to select clock frequency. (Jumper is inserted at 4 Hz position).

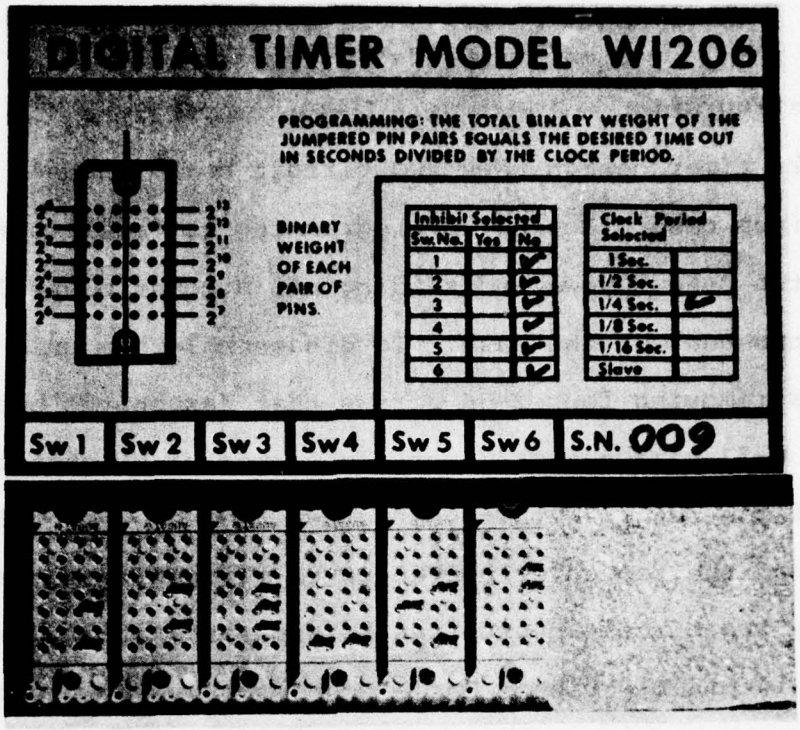


Figure 5a. Timer's label provides spaces to denote the features selected during fabrication plus instructions for programming the Timer.

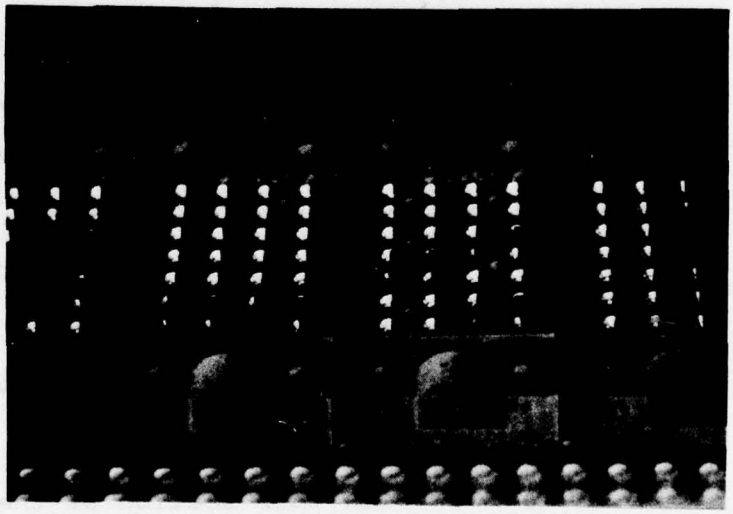


Figure 5b.

Augat #8136-651 P2 two pin connectors serve to tie counter outputs to NAND gate inputs thus programming the Timer.

Weight: Approximately 800 gms (1 3/4 lbs.)

Finish: Finish is gold irridite and white vinyl.

3.2 Configuration

This timer design uses two circuit boards housed within an aluminum case. Access to programming is facilitated by removing two 2-56 screws and sliding off a cover plate located at the top rear of the case. To disassemble the unit further requires removing four 2-56 screws that fasten the back plate, and two 6-32 screws that mount the connector bracket to the front of the case. With these screws removed, both circuit boards and the top cover plate can be slipped from the case.

The two circuit boards can be separated after disconnecting the two 16 pin DIP ribbon cable connectors. The top circuit board (Figure 2a, 2b) uses wire-wrap and holds 28 DIP sockets, while the bottom board (Figure 3, 4a) is a two layer p.c. board with plated through holes.

Special patterns on the p.c. board allow the use of Augat #8136-651 P2 two pin connectors to jumper the inhibit lead of each output through to the Cannon DCC-37P Connector. These inhibit leads are brought out only if they are to be used. Otherwise, without the jumper installed, there is no external access to them. Another p.c. pattern (Figure 4b) is used to select one of five clock frequencies to be used by the timer. A label fixed to the top cover plate (Figure 5a) provides space to note the installation of these jumpers. It also identifies the programming sockets (Figure 5b) and provides brief instructions for programming the timer.

The photos with this section of the report illustrate these features.

4.0 THEORY OF OPERATION

The theory of operation can best be explained by using Figure 6 as a guide. The circuitry shown, though greatly simplified in this drawing, does accurately depict the design concept of this timer.

This design is made up of three basic elements: a counter, a programming device and a NAND gate. A NAND gate output switches from high to low when all of its inputs are high. In our example, the NAND gate inputs 1, 2, 3 and 4 are tied respectively to counter outputs 2^0, 2^1, 2^2 and 2^3 through the programming device represented here as a closed SPST switch. As NAND gate 5 is not tied to the counter, its input is held high continuously through its 220 KΩ pull up resister to V_{DD}. The inputs that are tied to the counter follow the counter output. Figure 7 shows a timing diagram of the counter's outputs. It can be seen that the outputs change status only on the negative going edge of the preceding signal. The result is a halving of the output frequency from one signal to the next. Each output is labeled with a value, in powers of two, that represents the number of clock periods contained within one half cycle of its output. The time out desired is obtained by summing together these numbers of clock periods represented by each counter output. Our example shows a time out of 15 counts (each count represents one clock period). Cross tying 2^0 (1 count) 2^1 (2 counts) 2^2 (4 counts) and 2^3 (8 counts) makes the total 15 counts. If, for convenience, we use a 1 Hz clock with a clock period equal to 1 second, our programmed time out will be 15 seconds.

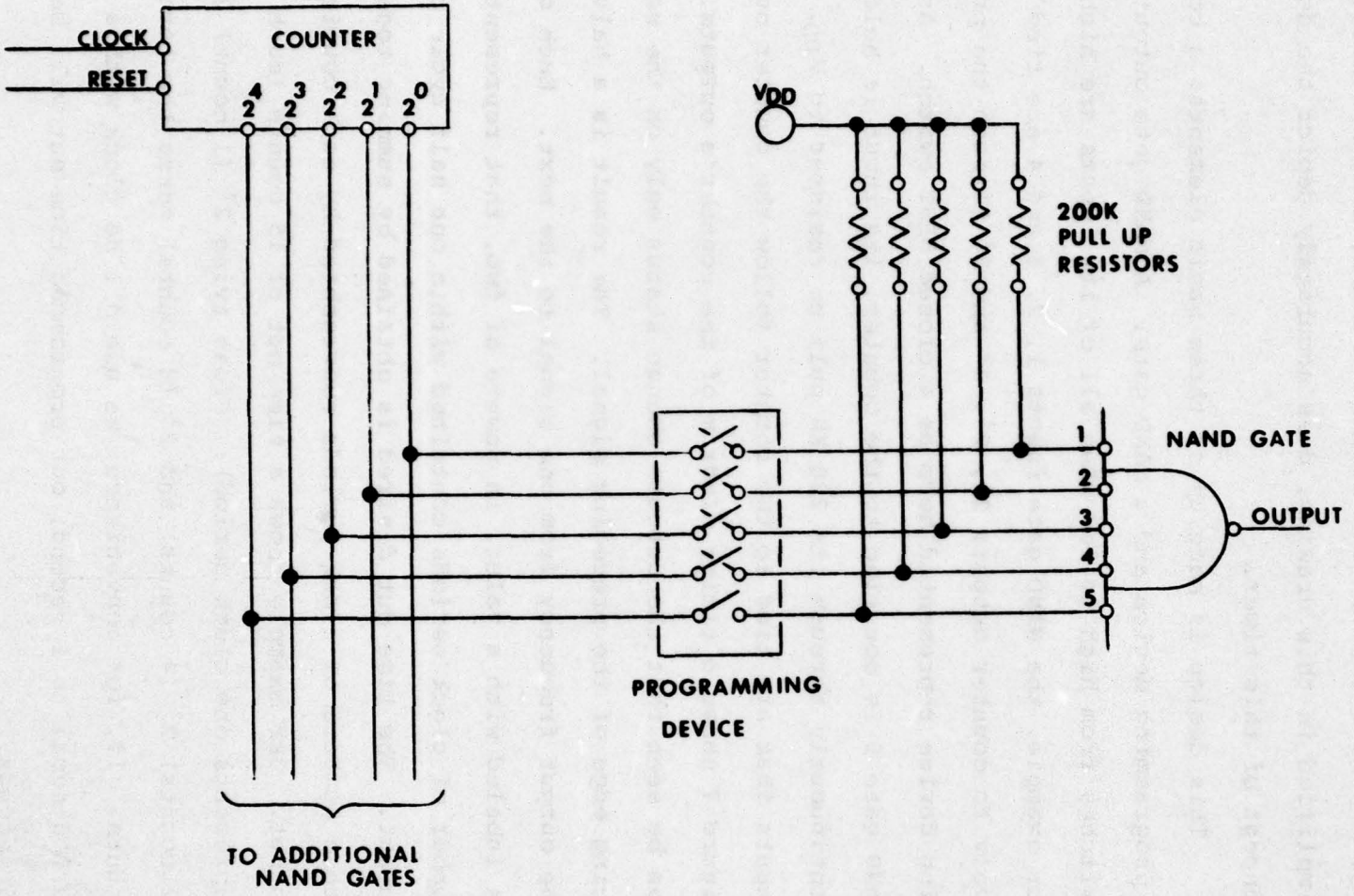


Figure 6. **DESIGN CONCEPT**

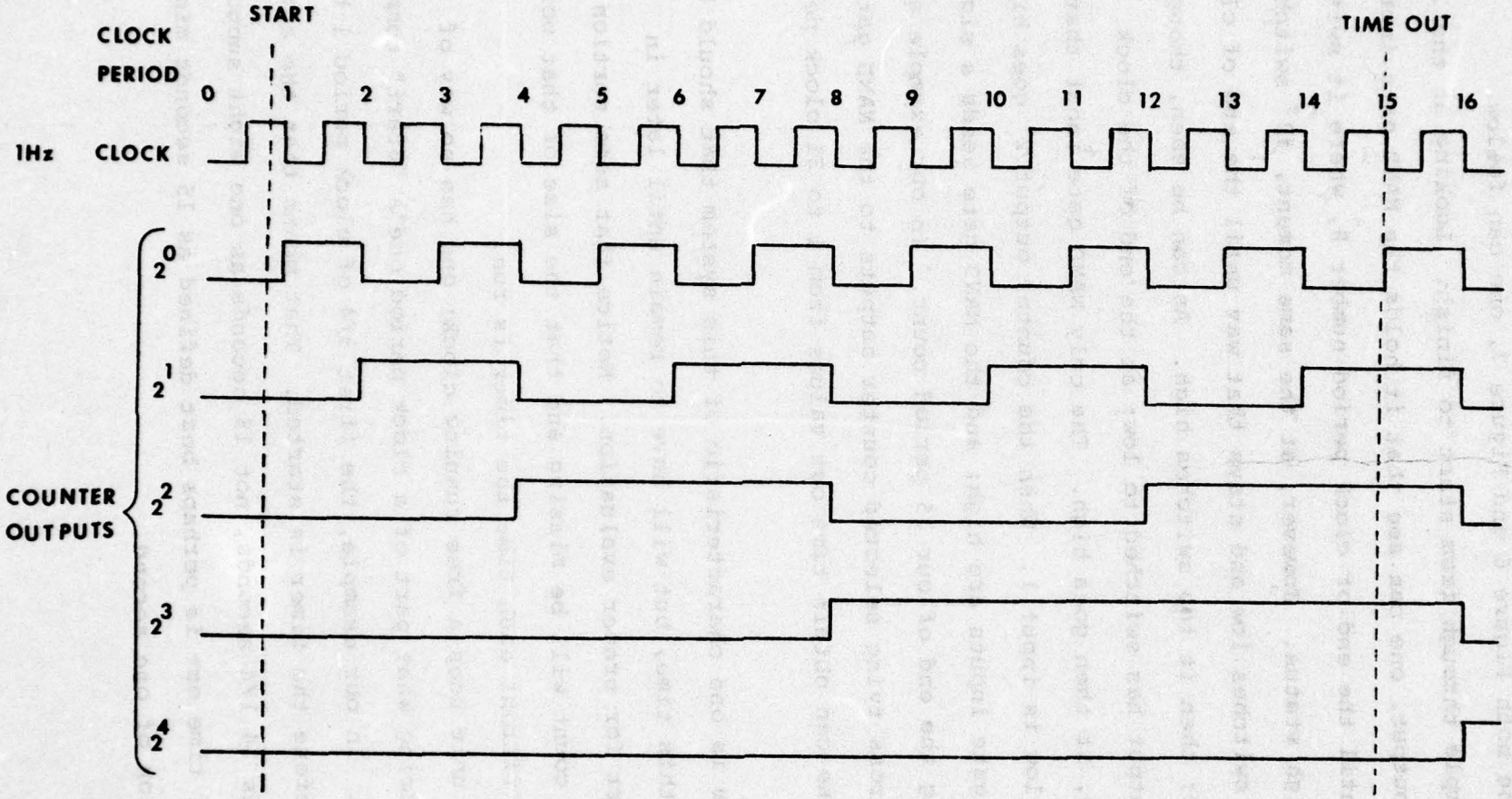


Figure 7. **TIMING DIAGRAM**

Using both Figure 6 and Figure 7, one can follow this example through from start to finish. Looking at the 2^3 counter output, one can see that it holds the NAND gate input 4 low, until the end of clock period number 8, where it switches to the high status. However, at the same moment, $\#2^3$ switches high, 2^2 switches low and stays that way until the end of clock period 12; then it too switches high. As can be seen, though, the 2^1 output has switched to low; at the end of the clock period 14, it then goes high. The only NAND gate input that is now held low is input 1. When the counter output 2^0 goes high, all NAND gate inputs are high; and the NAND gate sends a signal indicating the end of our 15 period count. In our example system, by cross tying selected counter outputs to the NAND gate inputs, one can obtain time out values from 1 to 31 clock periods maximum.

There is one characteristic of this system that should be noted at this time, but will have to remain until later in this report for proper evaluation. Notice that some portion of the first count will be missing and that the size of that portion will be different each time the timer is run.

This unit uses a free running clock; one has no way of knowing during what part of a clock period one's "Start" command will fall. In our example, the first 3/4 of clock period 1 has elapsed before the timer is started. That means that the actual time out is 14 1/4 seconds, not 15 seconds as one might suppose. The actual time out is perhaps best defined as 15 seconds minus some portion of one second.

5.0 CIRCUIT DESCRIPTION

The circuit used as an example in Figure 6 has a limited capability. The following description is of the actual circuitry used in the timer.

5.1 Counter (Figure 8)

The counter uses two CD 4024 AF seven stage binary ripple counters with the 2^6 output of the first supplying the clock input to the second. This combination gives fourteen counter outputs labeled sequentially, 2^0 to 2^{13} inclusive. The label indicates the total number of clock periods (or timing increments) contained in one half cycle of the labeled output.

5.2 Programming Device (Figure 9)

As in the example circuit, outputs from the counter go to a programming device (PSO-X01). A 28 pin Augat 528-AG26 F DIP socket is used for this purpose. Fourteen pairs of socket pins (one pair assigned to each of the counter outputs) act as SPST switches when jumpered with Augat 8136-651 2P two pin connectors. These switches when closed, tie the counter output leads to the NAND gate (IC-X02, -X03) inputs. Six of these DIP sockets, each wired in parallel to the counter output, allow independent programming of each of the timer's six outputs.

5.3 NAND Gate (Figure 9)

Each timer output requires two CD4068 eight input NAND gates, thus giving a total of 16 inputs. The two gates, IC-X02 and IC-X03, act as one (except for an inverted output) because their outputs are tied to the two inputs of a two input NOR gate (1/4 IC-07). Each NOR gate is one quarter of a

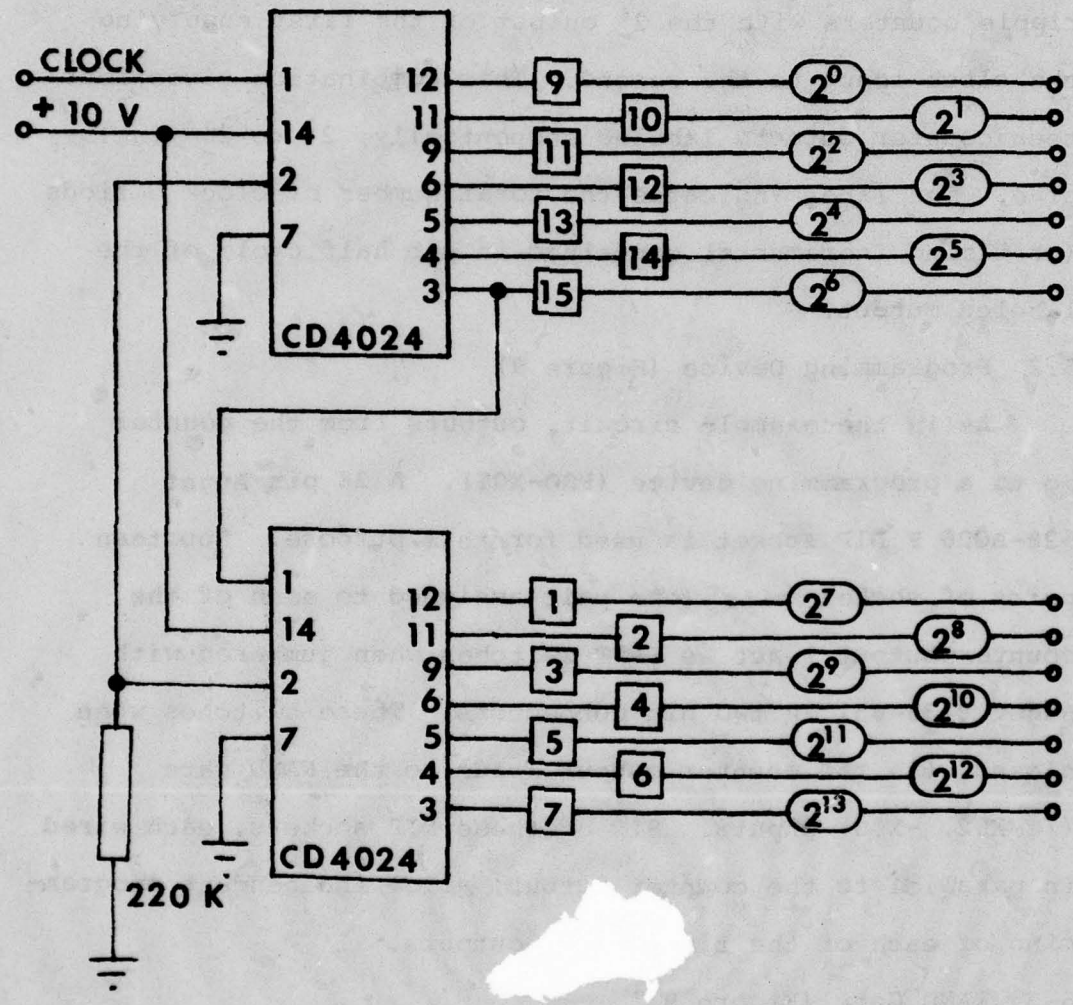


Figure 8. **COUNTER CIRCUIT**

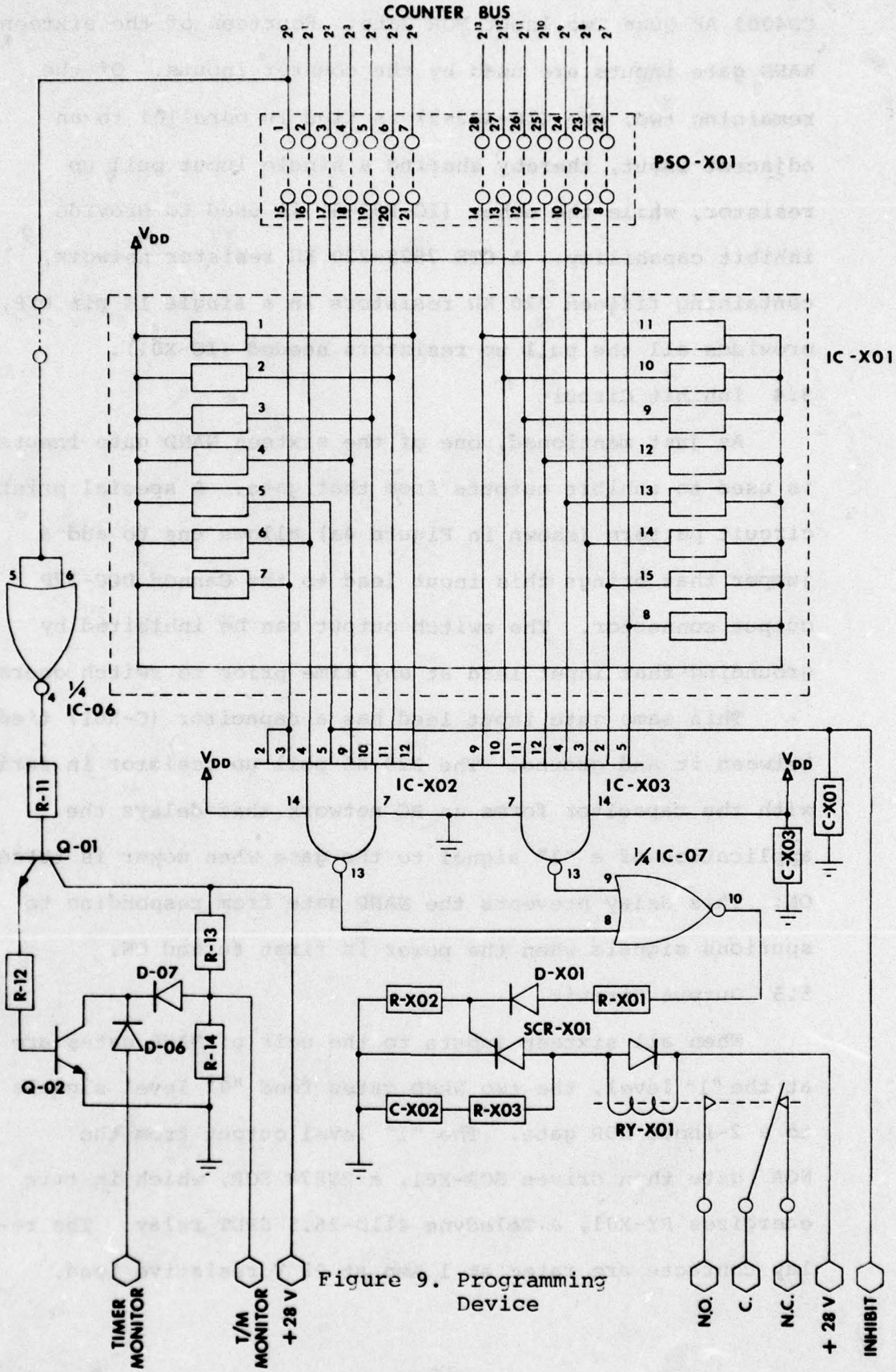


Figure 9. Programming Device

CD4001 AF Quad Two Input NOR Gate. Fourteen of the sixteen NAND gate inputs are used by the counter inputs. Of the remaining two, one (IC-X02-2) is tied in parallel to an adjacent input, thereby sharing a single input pull up resistor, while the other (IC-X02-5) is used to provide inhibit capability. A CTS 7625-220 KΩ resistor network, containing fifteen 220 KΩ resistors in a single 16 pin DIP, provides all the pull up resistors needed (IC-X01).

5.4 Inhibit Circuit

As just mentioned, one of the sixteen NAND gate inputs is used to inhibit outputs from that gate. A special printed circuit pattern (shown in Figure 4a) allows one to add a jumper that brings this input lead to the Cannon DCC-37P output connector. The switch output can be inhibited by grounding that input lead at any time prior to switch operation.

This same gate input lead has a capacitor (C-X01) tied between it and ground. The 220 KΩ pull up resistor in series with the capacitor forms an RC network that delays the application of a "1" signal to the gate when power is turned ON. This delay prevents the NAND gate from responding to spurious signals when the power is first turned ON.

5.5 Output Circuit

When all sixteen inputs to the pair of NAND gates are at the "1" level, the two NAND gates feed "0" level signals to a 2-input NOR gate. The "1" level output from the NOR gate then drives SCR-X01, a 2N878 SCR, which in turn energizes RY-X01, a Teledyne 411D-26.5 SPDT relay. The relay contacts are rated at 1 Amp at 28 V resistive load.

5.6 Monitor Circuits (Figure 9)

Two monitor circuits are used; one supplies a signal for T/M use, the other operates a lamp on the control console. They are generated by monitoring an appropriate counter output (1 or 2 Hz). This signal is inverted by a NOR gate (both inputs tied together) then fed to Q-01, an MPS-13A transistor which then drives Q-02, a 2N720A transistor. This transistor is used as a switch to ground for the monitor lamp on the control console and for a voltage divider network R-13, R-14 for T/M. Both monitors supply a steady output when the timer is "Reset" and a pulsating output when it is running.

5.7 Clock Circuit (Figure 10a)

The oscillator used is a Connor Winfield Model L24R1M set to 4.096 K Hz. Its frequency tolerance is ±0.005% with a temperature range of -40°C to 85°C. Five of its outputs are brought out to a printed circuit pattern where, by using a jumper, one has the choice of a 1 Hz, 4 Hz, 8 Hz or 16 Hz output frequency.

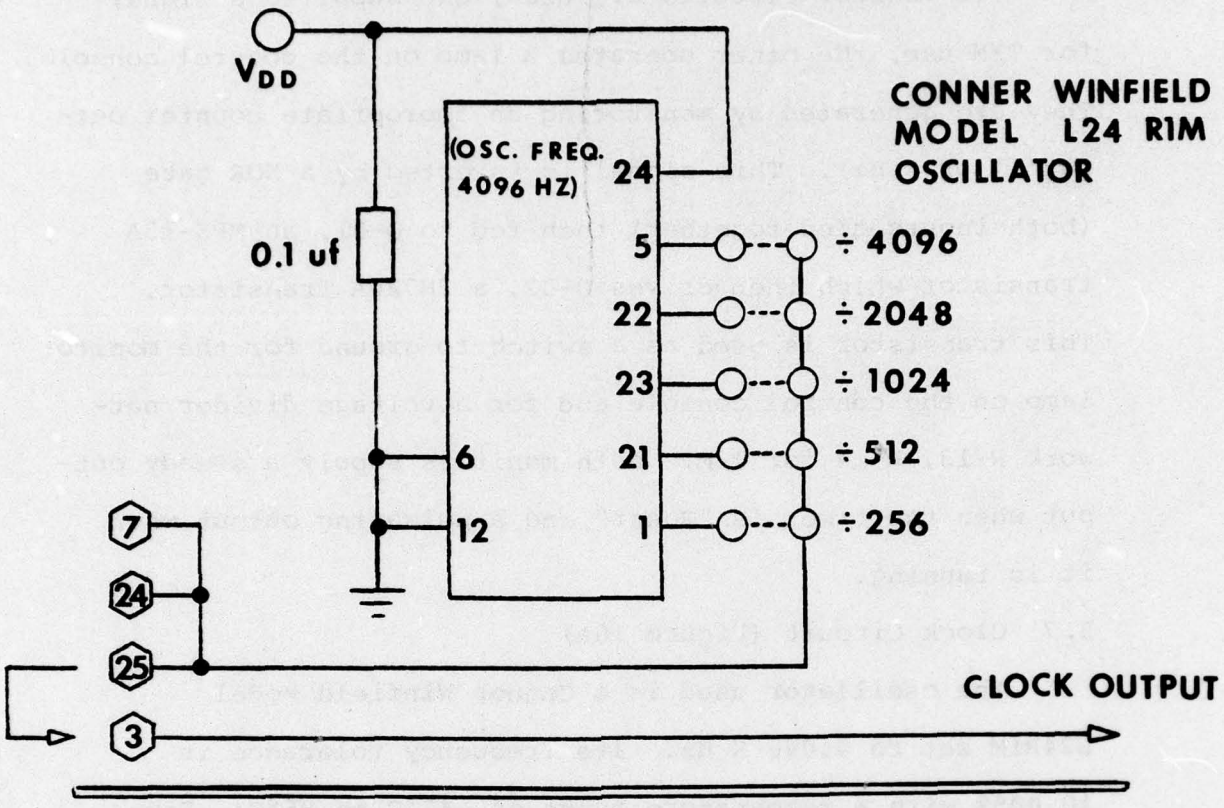
5.8 Reset/Start (Figure 10b)

A Teledyne 411D-26.5 relay is held in the "Reset" position by power from the control console. Disconnecting or interrupting the power allows the relay to drop out, thus starting the timing sequence. Re-energizing the relay resets the timer to its starting point by applying a command to the "Reset" inputs of both CD4024 AF counters.

5.9 Power Supplies (Figure 11)

Two μ723 voltage regulators are used to supply the timer with V_{DD} of + 10 VDC.

Figure 10a. **CLOCK CIRCUIT**



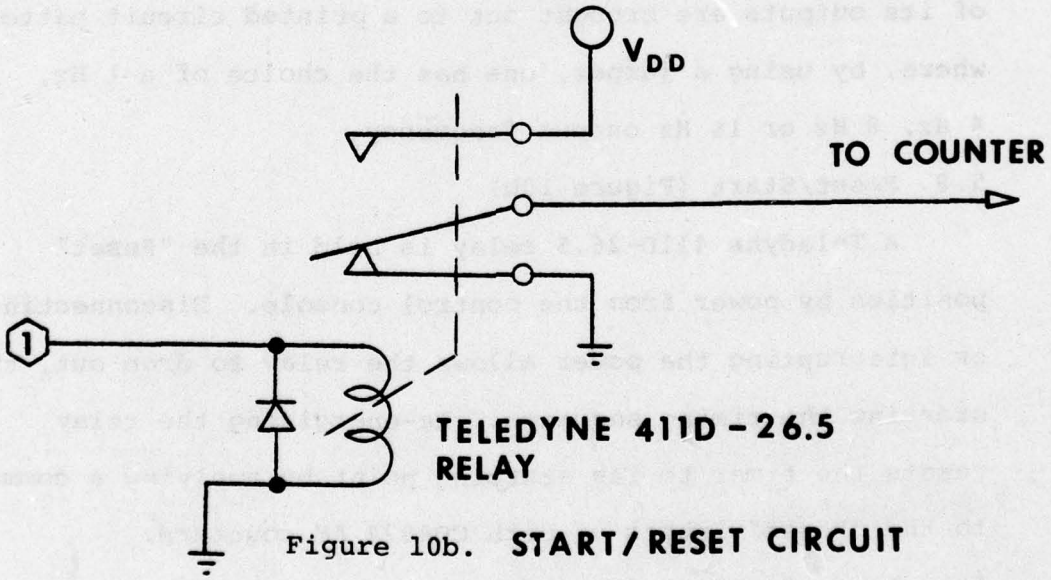


Figure 10b. **START/RESET CIRCUIT**

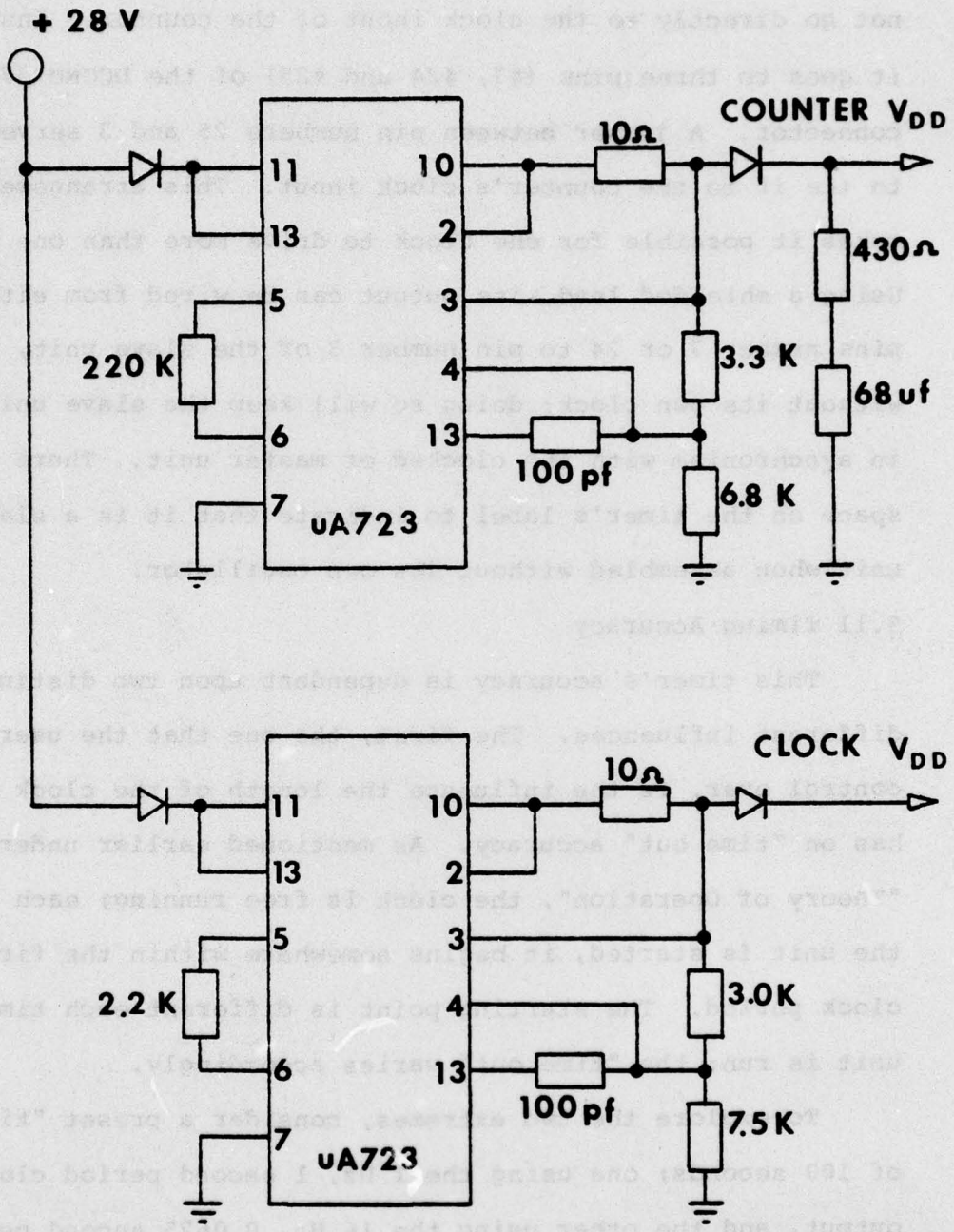


Figure 11. **COUNTER / CLOCK POWER SUPPLIES**

clock periods was required; therefore counter outputs 2^6, 2^5 and 2^7 must be programmed or added together to equal the 100 count. In the second case, a count of 1600 clock periods is required. Counter outputs 2^{10}, 2^9 and 2^6 must be added to equal a count of 1600 for the 100 second time out. It can be seen that "time out" accuracy can be improved by using the 16 Hz instead of the 1 Hz frequency. The 16 Hz frequency may be used, provided that all of the timer's outputs are under 1,024 seconds. If any of them exceed 1,024 seconds, then a lower clock frequency must be selected. Lowering the frequency increases the maximum "time out" value until at 1 Hz, a value of 16,383 seconds (>4½ hours) is reached.

Note that this source of error does not affect the time differences between the individual outputs of the timer. Those differences remain as programmed, except as they are influenced by the second source of timing error.

The second source of timing error is the clock. This timer uses a Connor Winfield model L24 R 1 M crystal oscillator, rated at a frequency tolerance of ±.005% when the temperature is within -40°C to +85°C and the input voltage is between +5 VDC to +15 VDC, regulated at ±5%. This type of error affects all timer outputs.

The combination of both types of error seldom exceeds the ±1% limit used as a design goal.

5.12 Programming

Programming the timer is accomplished by plugging two pin jumpers into appropriate sockets. The left side of the timer label (see Figure 5a) shows a graphic

reproduction of a programming socket. Using it as a reference, the following steps program the timer: (It is assumed that the clock period best suited to the application has been selected and hardwired in during the unit's fabrication. For this timer, it is 1/4 second.)

1. Divide the "Time Out" in seconds by the clock period in seconds to obtain the total number of clock periods.
2. Notice that the programming socket in the diagram is divided down the center and that each pair of pins, starting at the upper left, is labeled with a value defined by an exponential value of two. Proceeding C.C.W., the exponents run from 0 - 13 inclusive.

Label	Value	Label	Value
2^0	= 1	2^{13}	= 8192
2^1	= 2	2^{12}	= 4096
2^2	= 4	2^{11}	= 2048
2^3	= 8	2^{10}	= 1024
2^4	= 16	2^9	= 512
2^5	= 32	2^8	= 256
2^6	= 64	2^7	= 128

The value of each pin pair is shown above.

3. Determine which values when added together, equal the number of clock periods needed to equal the desired time out. Install two pin jumpers at each matching pin pair sockets.

In Figure 5a, the switches are programmed to:

*Switch #1, $2^7 + 2^9$ = 640 clock periods x ½ = 160 seconds

*Switch #2, $2^9 + 2^{10}$ = 1280 clock periods x ¼ = 320 seconds

*Switch #3, $2^8 + 2^9 + 2^{10}$ = 1792 clock periods x ¼ = 448 seconds

*Switch #4, $2^6 + 2^7$ = 192 clock periods x ¼ = 48 seconds

*Switch #5, $2^4 + 2^7 + 2^{10}$ = 1168 clock periods x ¼ = 292 seconds

*Switch #6, $2^{10} + 2^{11}$ = 3072 clock periods x ¼ = 768 seconds

* Switches, once closed, remain closed until timer is powered down.

6.0 SUMMARY

The Digital Timer Model W1206 satisfies the requirements of the SPICE, IRBS and ZIP programs. In fact, its programming ease and flexibility combined with the master/slave and inhibit features make it a likely candidate for use in most forseeable sounding rocket programs.

SPICE Sensor Deployment

1.0 INTRODUCTION

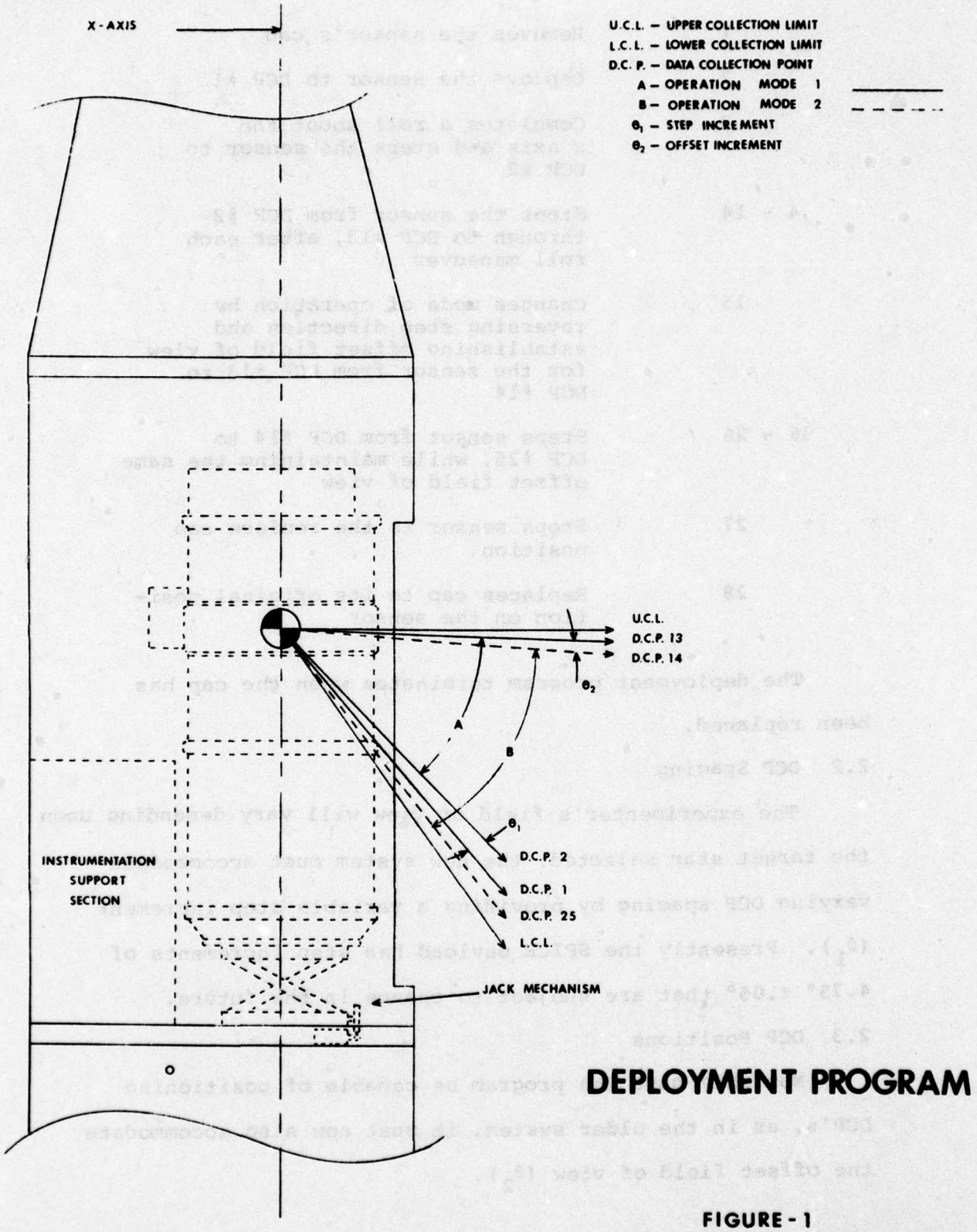
This report section describes the modifications made to the design and fabrication of a control system for the deployment of a cryogenically-cooled, infrared sensing instrument. The control system concept was originally used in the Hi-Star and Hi-Star South payloads. The successful performance of these payloads formed the basis for using this concept in the upcoming projects at Wentworth Institute. The new control system will differ from the previous system mainly because of the inertias involved and the deployment requirements. This new control system is presently being used in Project SPICE, and intended for use in Project ZIP.

2.0 CONTROL SYSTEM REQUIREMENTS

This control system has requirements similar to the previous control system; however, there are modifications to the sensor deployment program, data collecting point (DCP) spacing, and DCP positions.

2.1 Sensor Deployment Program

The new deployment sequence can be followed by referring to Figure 1. The unique features of this program in this sequence of events are that the system has two modes of operation -- mode #1 and mode #2; and that each mode of operation must be offset from the other. The following is the new sequence of events for the deployment program; it will be initiated by either the payload programmer or the A.C.S.



DEPLOYMENT PROGRAM

FIGURE - 1

Event #	Description of Events
1	Removes the sensor's cap
2	Deploys the sensor to DCP #1
3	Completes a roll about the x axis and steps the sensor to DCP #2
4 - 14	Steps the sensor from DCP #2 through to DCP #13, after each roll maneuver
15	Changes mode of operation by reversing step direction and establishing offset field of view for the sensor from DCP #13 to DCP #14
16 - 26	Steps sensor from DCP #14 to DCP #25, while maintaining the same offset field of view
27	Steps sensor to the replace cap position.
28	Replaces cap to its original position on the sensor

The deployment program terminates when the cap has been replaced.

2.2 DCP Spacing

The experimenter's field of view will vary depending upon the target star selected; the new system must accommodate varying DCP spacing by providing a variable step increment (θ_1). Presently the SPICE payload has step increments of 4.75° ±.05° that are subject to change in the future.

2.3 DCP Positions

Not only must the program be capable of positioning DCP's, as in the older system, it must now also accommodate the offset field of view (θ_2).

3.0 PHYSICAL DESCRIPTION

Since the sensor to be used in the SPICE payload is physically larger, both in size and weight, than in the Hi-Star and Hi-Star South systems, the payload structure and certain mechaisms have to be modified in order to accommodate it. The following section is a discussion of these modifications.

3.1 Payload Structure

The structure, which houses the sensor, should be extremely rigid in order to maintain alignment of the sensor with the rest of the payload. In order to accommodate the larger sensor required in SPICE, this structure will increase in size approximately 10 times. The inner cavity, where the sensor is stored, must have a surface that aids in maintaining cleanliness.

3.2 Gimbal System

The gimbal in the SPICE payload is different from the arrangement used in the previous Hi-Star systems. The SPICE system uses a support casting that is directly coupled to a set of gimbal shafts. The support casting, in turn, is fastened to the sensor's mounting flange. The ends of the gimbal shaft protrude through opposite sides of the structure. They are coupled to the gimbal drive assembly on one side, and the gimbal brake assembly on the other.

3.3 Gimbal Drive Assembly

This assembly, located in the drive quadrant of the payload structure, consists of a gear box, function cam, shaft encoder and precision pot.

Gear Box - The reduction ratio of the worm drive has been increased to 84:1, while the planetary gear motor reduction ratio has decreased to 30.7:1. The combination of these reductions and a decrease in motor speed, has decreased the velocity of the sensor travel to approximately 10°/sec when 24 volts is applied to the motor's armature.

Shaft Encoder - This device is the absolute optical transducer used in the previous systems. Anti-backlash gears have been retained and are used to couple the encoder to the gimbal's shaft. The encoder to gimbal's shaft ratio is 2.652:1. This increases the resolution of the encoder's output to .0165°/bit.

Function Cam - This cam is coupled directly to the gimbal's shaft; it actuates two switches (SW5 and SW6) in the control system. The 40° enable switch (SW4) has been eliminated. This was possible because this sensor's maximum angle of deployment is limited to 90° from the x axis, therefore the encoder no longer generates redundant data.

Precision Pot - This pot has been removed from the brake assembly and remounted on the gimbal assembly. It is geared up to a ratio of 23.33 times the gimbal shaft. As before, it provides a back-up analog signal that monitors shaft position.

3.4 Gimbal Brake Assembly

A power-to-engage friction disc type brake is coupled to the gimbal's shaft. The main purpose of this device is

to provide static braking of the gimbal system; it also aids in the dynamic braking action. The main characteristic change in the device is the increase from 75 lbs-in. to 300 lbs-in. of static torque when 28 volts are applied. This increase of torque increases the response time from 10 msec. to 45 msec. Since the main dynamic braking is accomplished by the Wave Shaper circuit and capacitor braking element, this increase in response time is of little concern.

3.5 LCU Package

Due to the fact that the control system requirements were modified and that certain components were obsolete, the decision was made to design and fabricate a new LCU package. This package, shown in Figure 2, has reduced the number of interface connectors from three to one, with a total number of 48 pin outs, as compared to the 70 pin outs of the old LCU package. This package contains three boards -- A, B and C. These boards can be identified as the following: board A, the processing unit; board B, the control sequencer; and board C, the I/O adapter. Ribbon cable and dip connectors were used to interconnect these boards. One can see from Figure 3a that board A is the top board. Figure 3b, an enlarged section, shows programming arrangements for matrix #1 and matrix #14.

4.0 CONTROL SYSTEM

A pair of block diagrams will be used to compare the previous system with the present. Figure 4 represents the previous system, Hi-Star series, while Figure 5 represents the present design layout SPICE series. A comparison of these diagrams shows that the

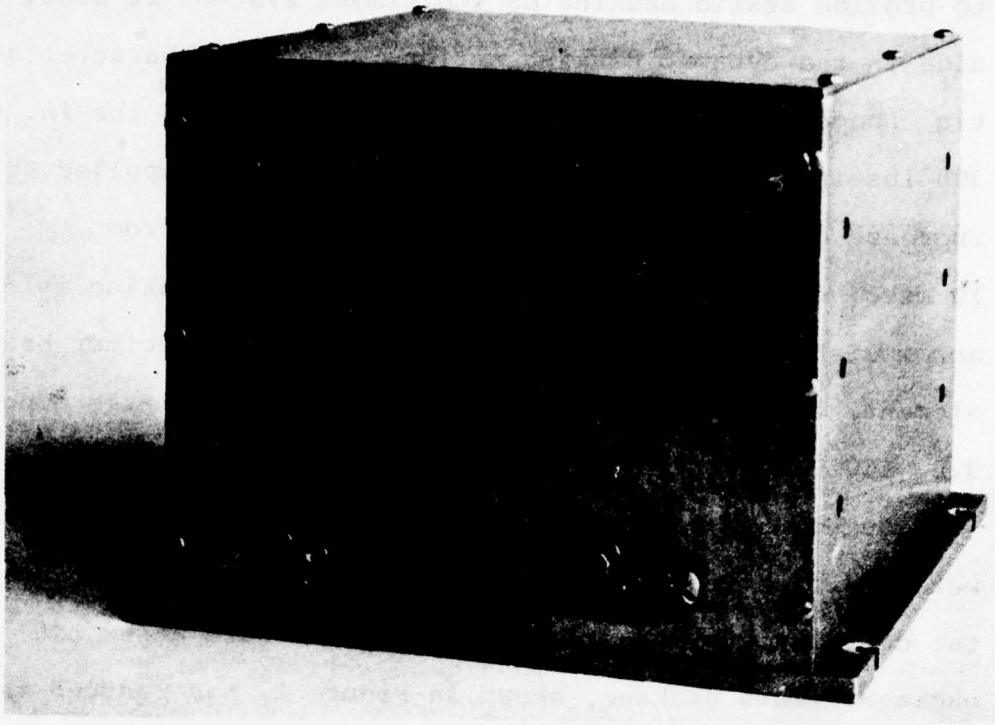
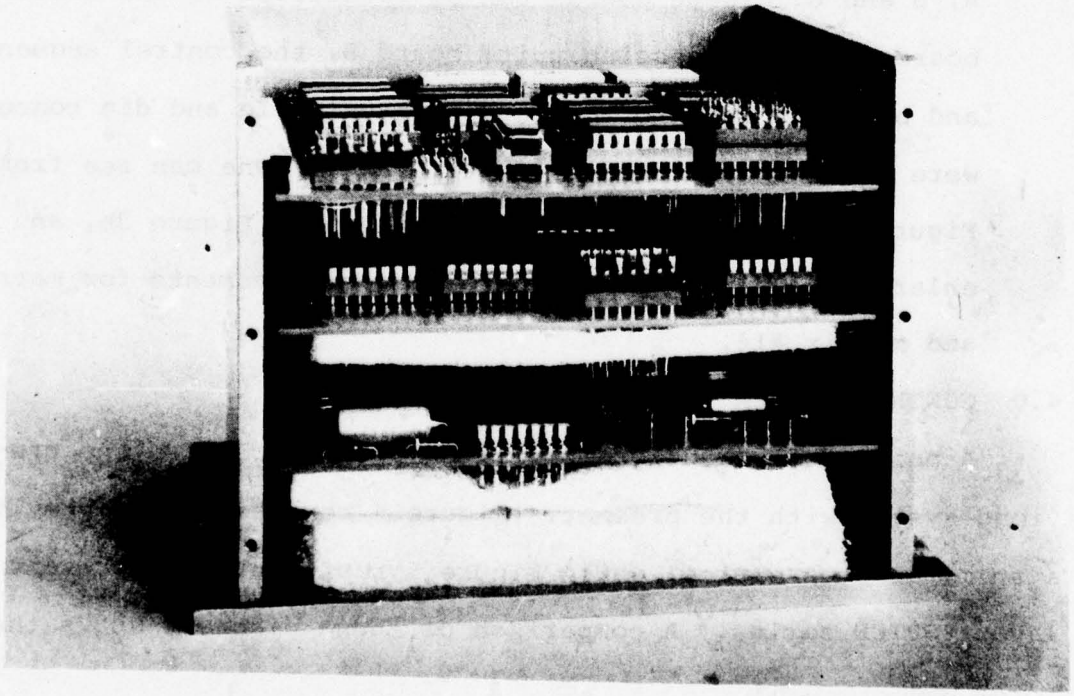


Figure 2. External and internal views of the Logic Control Unit (LCU) package



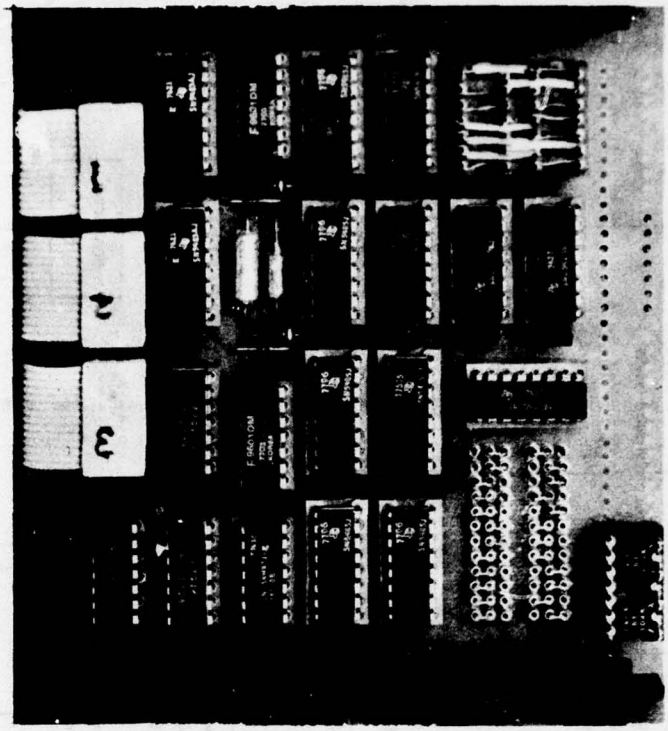


Figure 3a.

Board "A", one of three circuit boards in the LCU package.

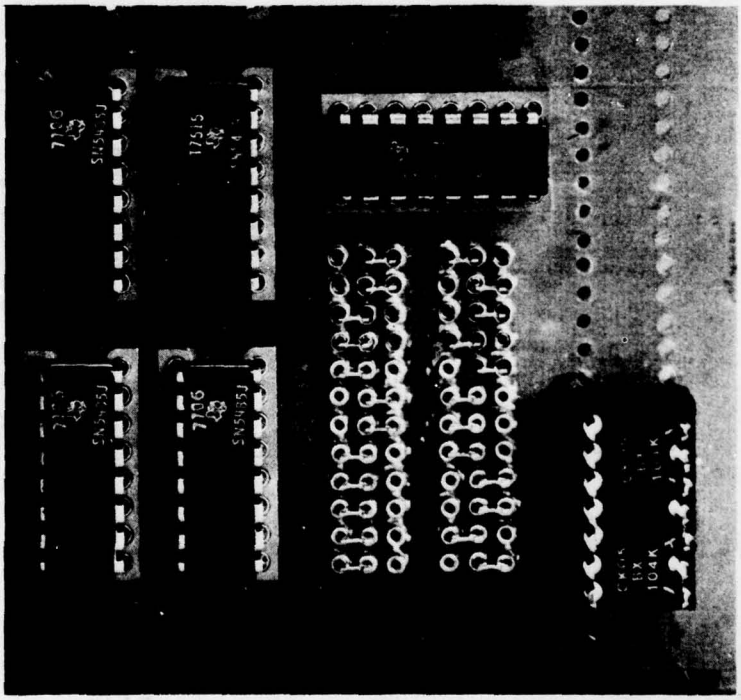
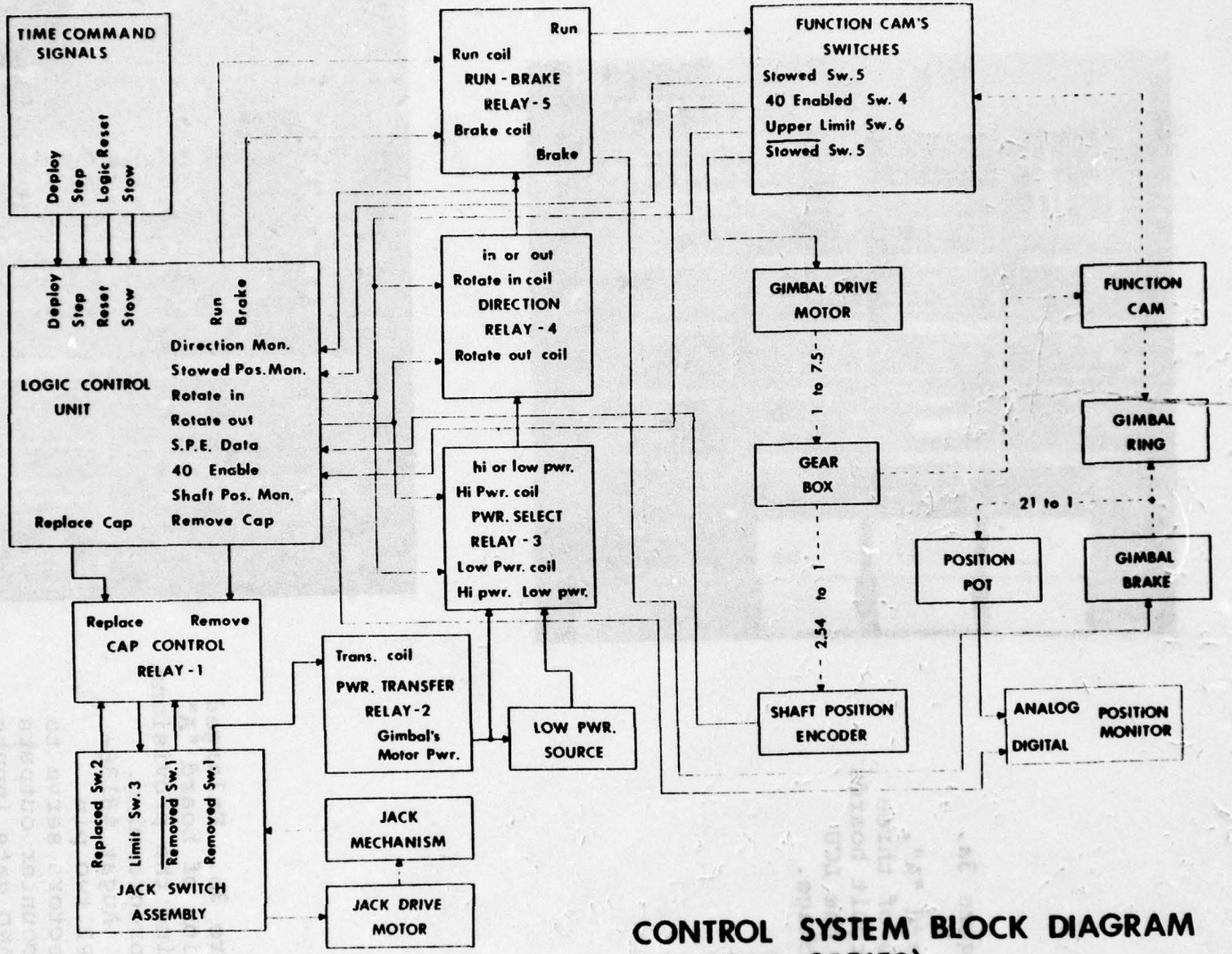


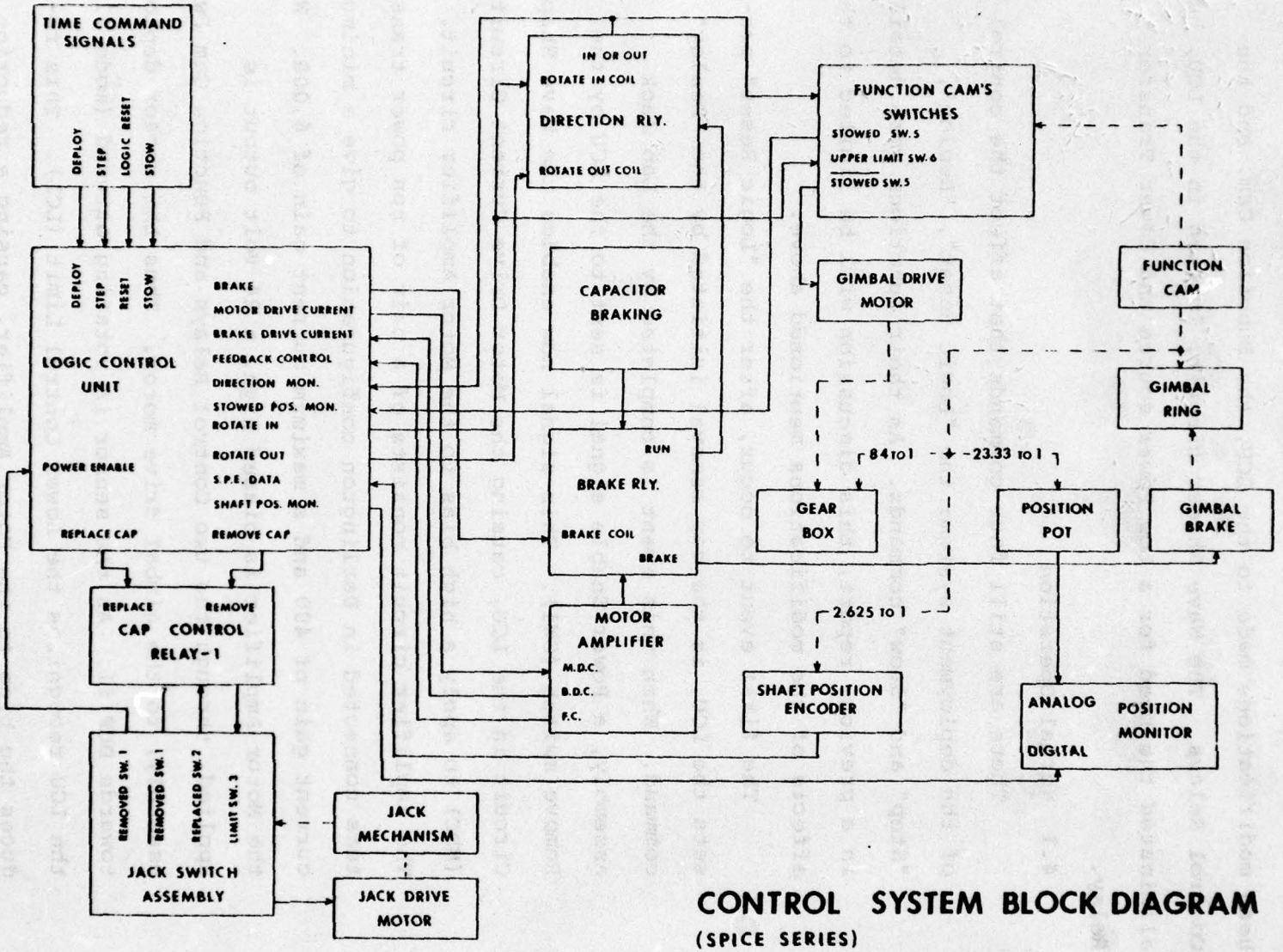
Figure 3b. Enlarged section of board "A" showing the provisions for programming.

Augat #8136-651 P2 two pin connectors serve to tie counter outputs to NAND gate inputs thus programming the Timer.



CONTROL SYSTEM BLOCK DIAGRAM (HI-STAR SERIES)

Figure 4.



CONTROL SYSTEM BLOCK DIAGRAM
(SPICE SERIES)

Figure 5.

present system has two new blocks -- a Motor Amplifier and a Braking Capacitor. A further comparison shows that there have been modifications made to the LCU, the Function Cam, and the Control Relays. The Wave Shaper circuit, located in the LCU, has eliminated the need for a Low Power source and Power Transfer Relay.

4.1 Normal Operation

There are still four commands that affect the control of the deployment system: the "Logic Reset", "Deploy", "Step" and "Stow" commands. As their functions were detailed in a previous report, this discussion will be limited to the effects of the modifications mentioned above.

The first event to occur, after the "Logic Reset" presets the LCU, is the cap removal initiated by the "Deploy" command. When this event is completed by the Lab Jack assembly, a *Power Enable* signal is sent to the LCU by the Remove switch (SW1). This signal now enables the Wave Shaper Circuit in the LCU, causing the Motor Drive Current Circuit (MDC) to apply a high bias to the Motor Amplifier circuit. The amplifier circuit consists of a pair of npn power transistors connected in Darlington configuration to give a minimum current gain of 400 and a maximum current gain of 6,000. When the Motor Amplifier is biased high, a 24 volt output is applied, through the two Control Relays and Function Cam Switch assembly, to the gimbal drive motor. Thus the sensor deploys towards DCP #1. As the sensor is rotating outward (mode #1), the LCU recognizes the Lower Control Limit (LCL). This reduces the bias to the Motor Amplifier, causing a reduction to the drive motor. The sensor continues to rotate-out at

a reduced voltage level, until the LCU recognizes the coincidence point for DCP #1.

Any time the LCU recognizes a coincidence point for the DCPs, the following sequential events occur. The Motor Amplifier is biased off and the brake current drive (BCD) generates the initial dynamic braking action by sinking current from the pair of pnp power transistors located in the Motor Amplifier circuit. Also, at coincidence, a brake control signal is transmitted to the non-latching Brake Relay. Approximately 7 msec later, the actual contact transfer is established that aids in the dynamic braking action. This transfer of contacts disengages the armature leads of the motor from the Motor Amplifier and a potential of opposite polarity is now applied to this armature by the Capacitor Braking element, a 500 μf capacitor. Also, at transfer, 28 volts is applied to the gimbal brake, which takes approximately 28 msec. to engage from the time of actual coincidence. Thus the total elapsed time from coincidence to sensor stopping of approximately 30 msec., correlates into inherent maximum difference of .048° (or 3 bits) from the DCP #1. The Brake Relay will remain energized, allowing the sensor to gather data, until a "Step" command is generated by the ACS.

The "Step" command initiates a step operation which can be divided into three sequential segments: 1 - the step set; 2 - the time delay; 3 - coincidence recognition. All subsequent "Step" commands will initiate the same sequential segments, except for the last "Step" command in the mode #1

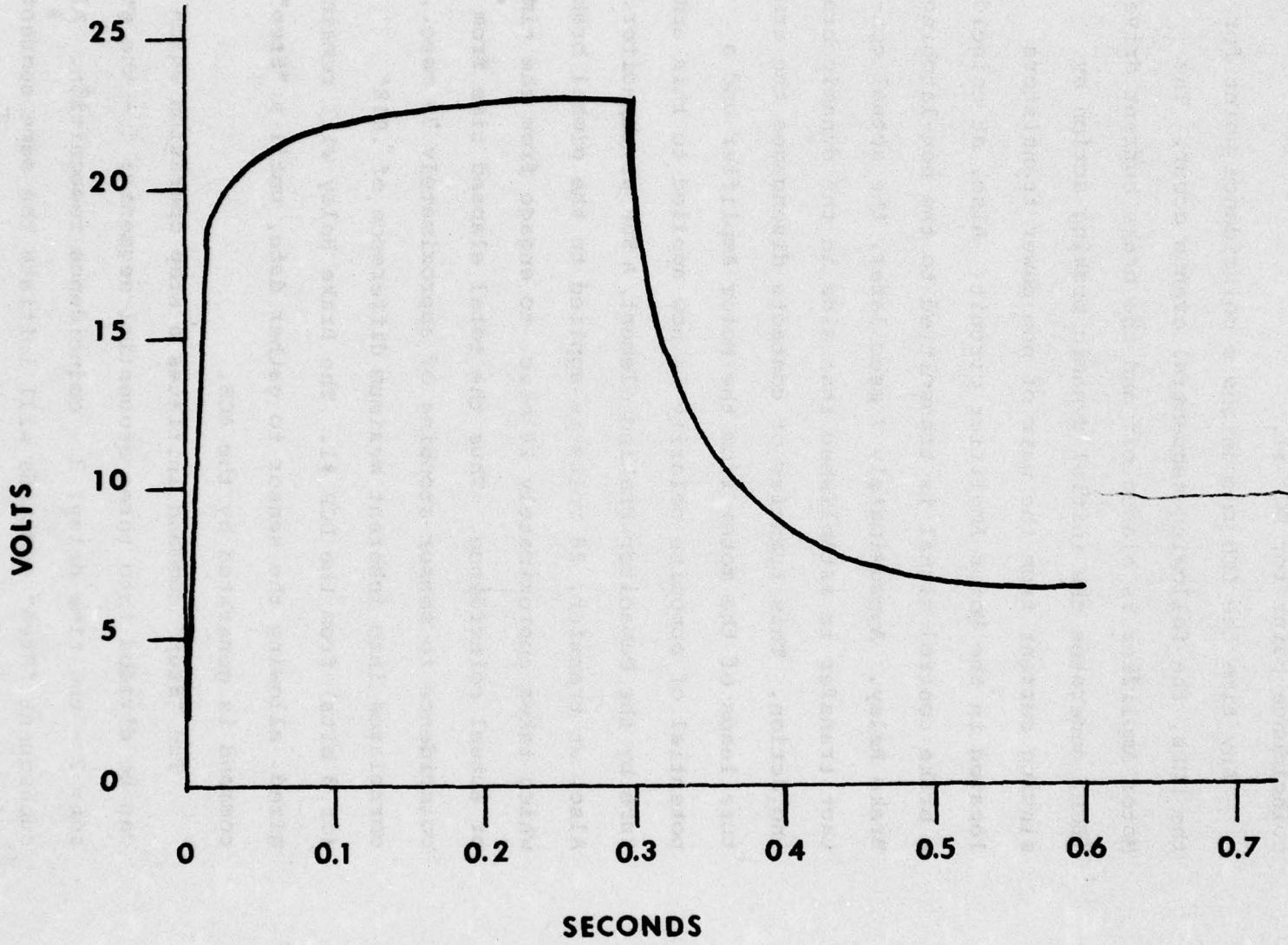


Figure 6. **STEP OPERATION VOLTAGE WAVEFORM**

operation. The armature's applied voltage wave form, Figure 6, can be used to follow each segment of the Step Operation.

The step set, segment 1, causes the LCU to transmit a high bias level to the Motor Amplifier; it also removes the brake control signal from the Brake Relay. When contact transfer has been established, the Braking Capacitor is recharged to a 28V potential, preparing it for the next dump discharge. Also, at contact transfer, the armature leads are reconnected to the Motor Amplifier. The armature now obtains a 24 volt potential before the time delay, segment 2, initiates its signals. At this time, approximately 300 msec. from step set, a new reference voltage ($Vref_2$) is generated within the LCU, causing a reduced bias level to appear on the motor drive output. This, in turn, causes an exponential decay of voltage on the armature. It takes approximately 200 msec. to decay to a 7 volt level. This voltage level will be maintained until the coincidence point for DCP #2 is recognized by the LCU. The time delay and the reduced voltage level are adjustable parameters within the Wave Shaper circuit. They can be varied to give the desired step performance. As mentioned before, a recognition of any DCP coincidence by the LCU will initiate signals to dynamically brake the drive motor.

After step operations, DCP #1 to DCP #13, have been completed, the Upper Control Limit (UCL) is recognized by the LCU. When this recognition occurs, a control signal is sent to the direction mode selector circuit within the LCU, causing signals to be transmitted from the LCU to the

Direction Relay. The sensor now rotates inward (mode #2) to DCP #14. When the sensor stops at DCP #14, the offset view angle, θ_2, has been established. Subsequent "Step" commands will now step the sensor inward to DCP #25. At DCP #25, the sensor will maintain its position until the LCU receives a "Stow" command from the payload programmer.

The "Stow" command generates two control signals. It also removes the brake control signal from the Brake Relay. The two control signals generated are the rotate-in signal, sent to the Direction Relay, and the high bias signal, sent to the Motor Amplifier. All other output controls are inhibited, with the exception of the replace cap control, thus allowing the sensor to rotate inward to the Stow position. Upon arrival at the Stow position, the replace cap control is initiated, causing the Lab Jack to replace the cap on the sensor. The completion of this event heralds the completion of the deployment program's Normal Operation.

4.2 Failsafe Operation

This control system still incorporates the two Failsafe modes of operation used previously, with essentially no change in their function and operation. (A full description of the scan mode and the lower limit control can be obtained from Campbell, Thomas J., Wentworth Institute of Technology, Boston, Massachusetts; "Rocket-borne IR Sensor Deployment", AFGL-TR-76-0125, 31 March 1976).

5.0 LCU

The composition and function of the LCU has been modified to accommodate the new deployment program and to improve motor control. These modifications required the addition of three

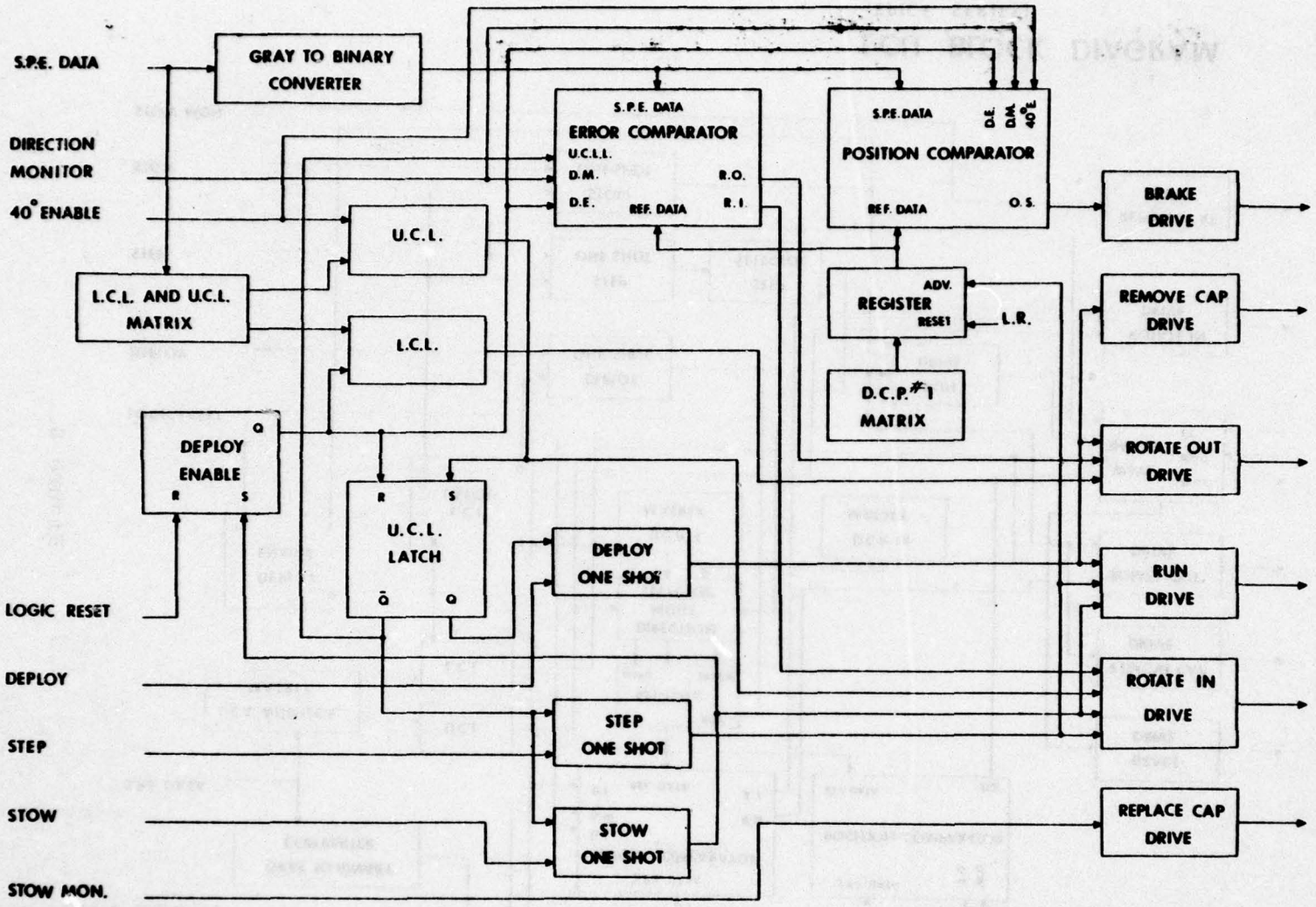
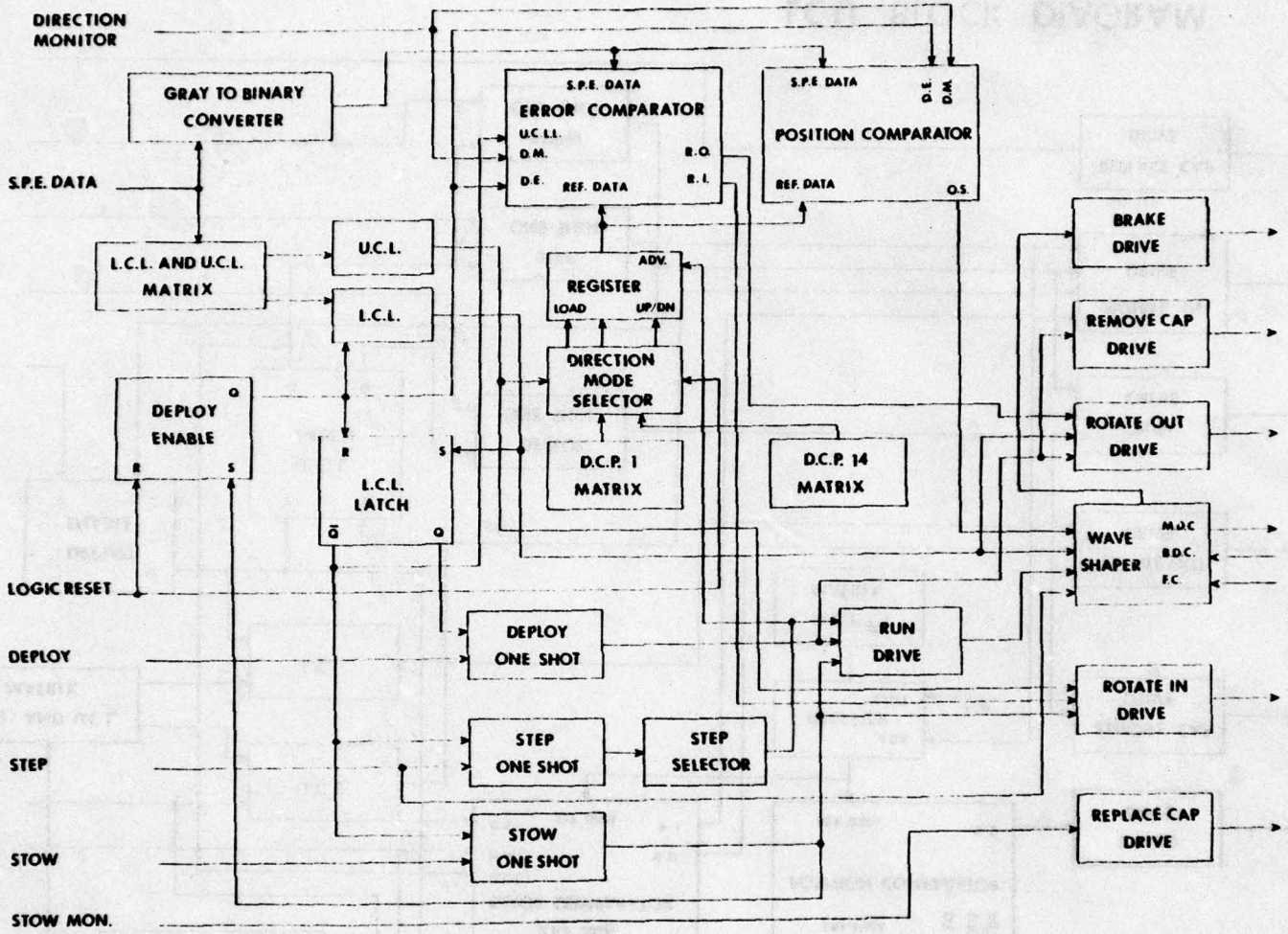


Figure 7.

LCU BLOCK DIAGRAM
(HI-STAR SERIES)



LCU BLOCK DIAGRAM
(SPICE SERIES)

Figure 8.

new circuits. A comparison between the old LCU block diagram, Figure 7 and the new block diagram, Figure 8, shows the addition of a Wave Shaper, Direction Mode Selector (DMS) and Step Selector circuit. All other circuit elements and functions remained unchanged, except for the composition of the register and comparator circuits.

5.1 Composition and Function

The Wave Shaper circuit can be divided into several smaller circuits -- a run-brake latch, a time delay, a Hi-$\overline{\text{Hi}}$ latch, a voltage regulator ($Vref_1$), a low voltage source ($Vref_2$) and a differential amplifier. The wave shaper circuit interfaces four input control signals with the Motor Amplifier; it also improves the control of the drive motor. The Run Drive and the Position Comparator circuits interface with the run-brake inputs of the Wave Shaper. These input controls determine whether the Motor Drive Current or the Brake Drive Current are biased on. The lower control limit (L.C.L.) and the step one-shot circuits interface with the time delay inputs of the Wave Shaper. A signal from either of these circuits will initiate a time delay that determines how long a high bias will appear on the Motor Drive Current output. The effects of the Wave Shaper circuit on the voltage applied to the armature during a step operation is illustrated in Figure 6.

The Direction Mode Selector circuit is comprised of 3 - 4 bit data selectors, word - direction latch, and a pair of one-shots. It interfaces the DCP #1 and DCP #14 with the register; and also provides a reset control signal

to the register. The control input signal for the Direction Mode Selector comes from the "Logic Reset" and the upper control limit (U.C.L.). The function of the Direction Mode Selector is to determine which mode the deployment system should be operating in.

The Step Selector is a programmable pulse generator that can produce up to 256 pulses. It interfaces the step one-shot with the register and run drive circuits. The addition of this circuit provides the control system with the means of varying the size of the increment angle (θ_1). The step increment angle can consist of a multiple of 0.033° with a maximum of 256 for an angle of 8.448°.

6.0 RESPONSE TO SYSTEM COMMANDS

The LCU responses to system commands have been explained in detail in Scientific Report #3. The following section will describe the reaction of the new components to certain system commands.

The "Logic Reset" affects the direction mode selector (D.M.S.), causing within the D.M.S., a reset of the word - direction latch and a triggering of the register load one-shot and word clock one-shot. When the latch is reset, the register receives a control signal that sets its mode of operation to the down direction. A reset of the latch also instructs the data selector within the D.M.S. to accept data from the DCP #1 Matrix, after it receives a pulse from the word clock one-shot. The register load one-shot generates a pulse and sends it to the register's load pin, thus allowing DCP #1 data to be stored in the register from the data select circuit. The sequence described above is

the reaction to the "Logic Reset" command, which essentially establishes the proper starting states for the various elements within the Direct Mode Selector and register circuits.

The deploy one-shot is triggered by the "Deploy" command, causing a run drive signal to be transmitted to the Wave Shaper circuit. This signal, in turn, generates within the Wave Shaper control, signals for the run-brake latch. The run-brake latch will be set to the run mode, activating an adjustable voltage regulator that is set to voltage reference #1 ($Vref_1$ = 12V). This source is connected to one input of the differential amplifier, and is also used as a source voltage for voltage reference #2 ($Vref_2$). The other input to the differential amplifier, $Vref_2$, is controlled by the Hi-$\overline{\text{Hi}}$ latch. The run drive signal sets this latch to the Hi mode, causing $Vref_2$ to be at ground level. When these latches are set to the run and Hi modes, a high voltage level appears on the Motor Drive Current (M.D.C.) output. This voltage level $VO = 2(Vref_1 - Vref_2)$, initiates the deployment sequence by applying a 24V signal to the motor amplifier. This signal level will be maintained until the lower control limit (L.C.L.) circuit sends its control signal to the Wave Shaper. An adjustable time delay, used mainly in the step operation, is activated by this signal. Upon completion of the time delay, the Hi-$\overline{\text{Hi}}$ latch will be set to the $\overline{\text{Hi}}$ mode. With this latch set in this position, $Vref_2$ now sources 8.5 volts to the differential amplifier, causing its output to be reduced to 7 volts. The recognition of DCP #1, by the position comparator, causes the run-brake latch to be set to the brake mode. The regulator is now turned off, setting $Vref_1$ and $Vref_2$ to

ground level. With the source voltages off, the Wave Shaper's brake drive current (B.D.C.) output provides a control signal that initializes the dynamic braking action. The completion of this action establishes DCP #1 in the deployment program. The LCU is now ready to accept a step command from the ACS programmer.

The "Step" command starts the step operation, by triggering both the step one-shot and time delay within the Wave Shaper. The output of the step one-shot activates the step select circuit. Pulse generated by this circuit updates the register information and triggers a control signal from the run drive circuit. The Wave Shaper input controls are now set to run and Hi mode. With the controls in this state, the voltage level on the M.D.C. will be at a high level until the time delay has elapsed. For the SPICE payload, this time delay is set for 300 msec., at which time the $\overline{\text{Hi}}$ mode is selected within the Wave Shaper. The control inputs, now set for run - $\overline{\text{Hi}}$ mode, cause the M.D.C. to decay to 7 volts. The coincidence point is established by the Shaft Position Encoder (S.P.E.) and the interaction of the following circuits -- Binary Converter, Position Comparator Register, Wave Shaper and Brake Drive circuits.

The S.P.E. transmits, in gray code, 13 bits of angular position data, of which the 12 most significant bits are transformed into binary data by the converter circuit. This positional data will be compared with DCP #2 data, which was updated in the register. When a match occurs, the position comparator's output will trigger the brake control input of the Wave Shaper. The triggering of this input activates a control signal for the

brake drive circuit which in turn, energizes the Brake Relay. Within the Wave Shaper, Vref1 and Vref2 sources are forced to ground level again, initializing the dynamic braking action. The completion of this action terminates the step operation for DCP #2. Subsequent step commands will provide the same sequential actions until the Upper Control Limit (U.C.L.) circuit identifies S.P.E. data that corresponds with the programmable U.C.L. matrix.

The recognition of the Upper Control Limit will initiate a control signal from the U.C.L. circuit that instructs the LCU to acquire DCP #14. This is accomplished by setting the Direction Mode Selector's (D.M.S.) word - direction latch to up mode and triggering the rotate-in drive circuit to the on state. With the D.M.S. circuit in the up mode, the register will contain data from the DCP #14 matrix and the direction of count for the register will be up. The signal from the rotate-in circuit causes the direction relay to change state, instituting a new direction of travel (Mode #2) for the sensor. The coincidence point, DCP #14, establishes the offset (θ_2) in the deployment program. The step increment (θ_2) and step operation will remain the same as in mode #1. The sensor will proceed to step inward to DCP #26; at this point, a "Stow" command will be generated by the payload programmer.

The "Stow" command will perform the same inhibit functions as in the previous LCU and cause the Wave Shaper to assume the run-hi modes of operation. This allows the sensor to deploy inward to the stow position. When the stow position is realized, the Replace Cap Drive circuit is triggered, causing the Lab Jack to replace the cap. The completion of this action terminates

the deployment program.

7.0 CONCLUSION

The modifications that were incorporated into this control system have produced a more versatile and controllable system. A large variety of deployment programs may now be implemented without major hardware changes. Added features, such as the bi-directional step program, programmable step angle (θ_1) and selectable offset angle (θ_2) have increased the system's versatility, while increased detection and braking capability combined with voltage wave shaping have improved system control. It is believed that future projects such as ZIP, requiring a similar deployment program, can readily adapt to this system without major design changes.

Rocket-borne Vibration Recorder (ROVIR)

1.0 INTRODUCTION

Airborne-type recording systems exist for use in aircraft and satellites for data recording. As such, these devices are expensive. A recording system, suitable for use in sounding rockets and also low cost, was not available.

In March of 1976, Wentworth Institute of Technology was asked by AFGL's Aerospace Instrumentation Division to design and build a suitable low cost system.

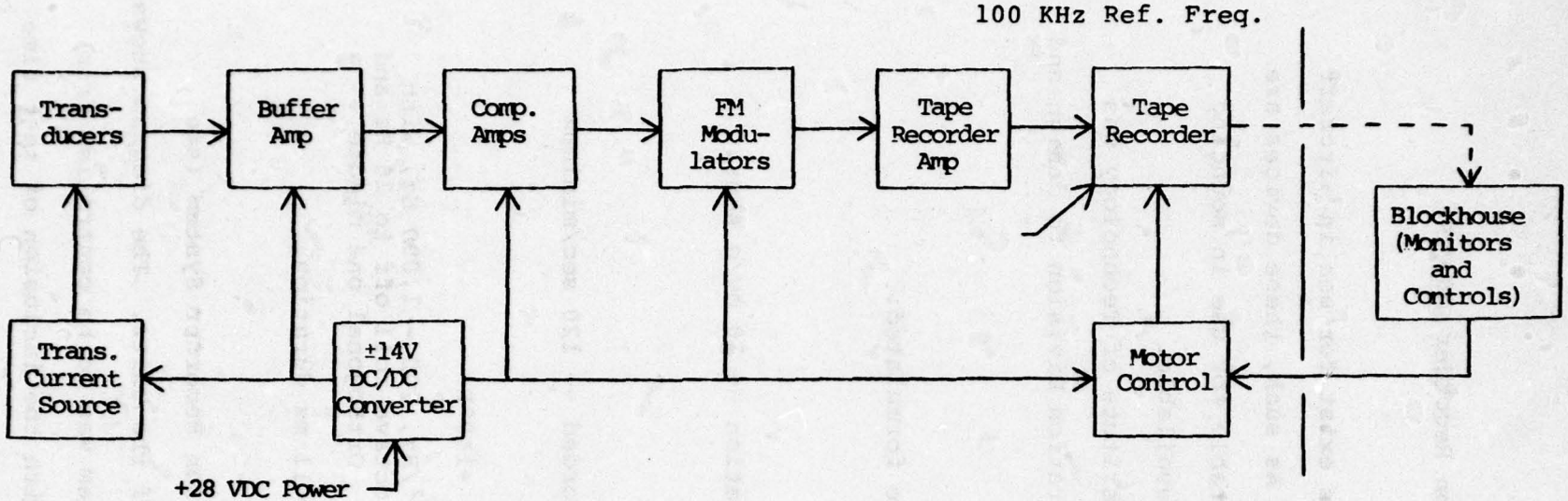
2.0 DESIGN REQUIREMENTS

The following requirements were formulated:

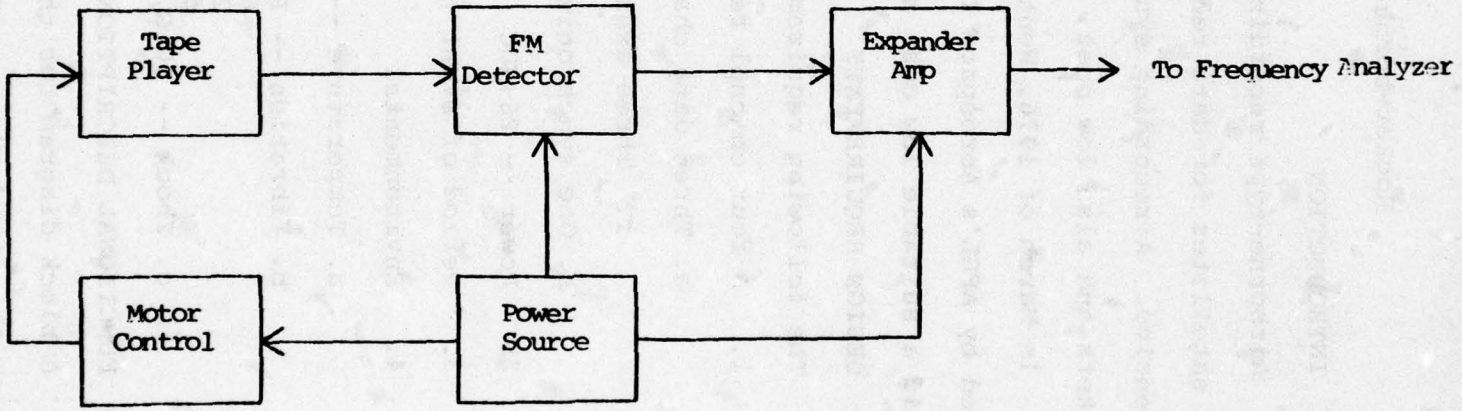
1. A four channel recorder
   a. Three data channels
      1. Three axes of vibration -- 10 mv/g sens.
   b. One synchronization
2. Power -- 28 VDC ±4 VDC
3. Period of event to be recorded -- 120 sec/minimum
4. Environmental
   a. Temperature -- -40° to +140°F
   b. Vibration -- PSD .15 G^2/Hz, 100 - 1,000 Hz, with 6 db per octave roll off to 20 Hz and 2,000 Hz. Orthogonal one minute duration.
   c. Shock -- 50 G, ½ sine, 11 ms duration.

3.0 FUNCTIONAL DESCRIPTION

A block diagram for the Vibration Recorder System (see Figure 1), shows the organization of the units. The diagram shows that the Vibration Recorder subsystem was to be controlled from the block house prior to launch. With the inclusion of test time



Vibration Recorder Subsystem Diagram



Vibration Playback Diagram

Figure 1. Vibration Recorder System

and pre-launch turn-on added to the flight requirement (see Design Requirement 3), the capacity of the tape system was determined.

Block house controls would be necessary to power and monitor the operation of the system.

3.1 The DC/DC Converter

This unit would use the 28 V power source (Design Requirement 2) available and convert it to the ± 14 VDC needed for the amplifier and motor control voltage. All items in the subsystem would be powered from either 28 VDC or the ± 14 VDC supply.

3.2 Transducers

The transducers would be of prime importance to the data portion of the system (Design Requirement 1.A.1.); their sensitivity and output characteristic had to be defined for the remainder of the system. The expected "G" level is 0 - 20 "G's", typical of previous sounding rockets. Emphasis is placed on low level measurements.

A Bolt, Beranek and Newman Inc. (BBN) transducer was selected for the following reasons: it uses internal electronics (eliminates pick-up from moving cables and saves charge amplifier cost); it has overvoltage protection, both from large transient from the piezoelectric crystal and from the output lead; it has immunity to 120 V 60 Hz on the output lead; and it has a favorable price.

3.3 Tape Transport

The Triple I tape cassette deck was found to be the least expensive basic transport system. Prices from nine

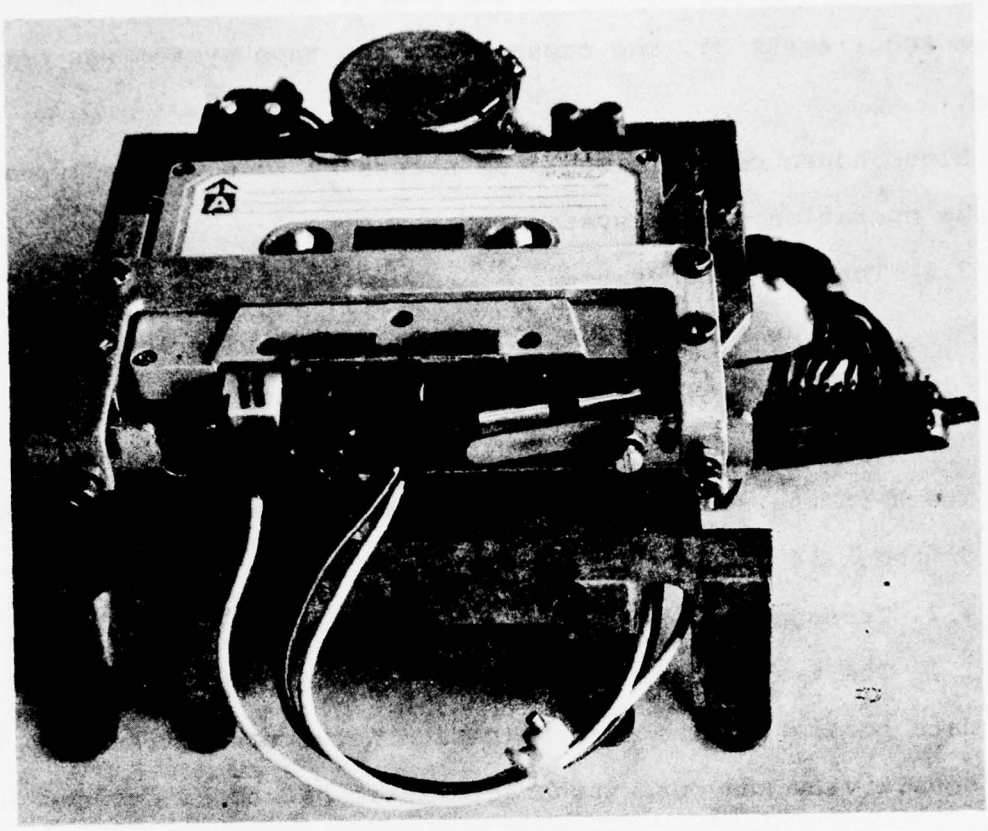


Figure 2. Top view of tape deck. Note brackets used to hold cassette securely into place.

companies ranged from $200. to $250,000. per system. Size and operating requirements were also considered. A Triple I, Phi-Deck variable speed deck was purchased.

The Unit had to be modified for environmental testing as follows:

A. A mechanical latch to keep the heads engaged and the cassette in place was fabricated. (See Figure 2.)

B. The Pulse generator, E.O.T. shut down feature, and recording prevention switch were removed. These features were not going to be used in flight.

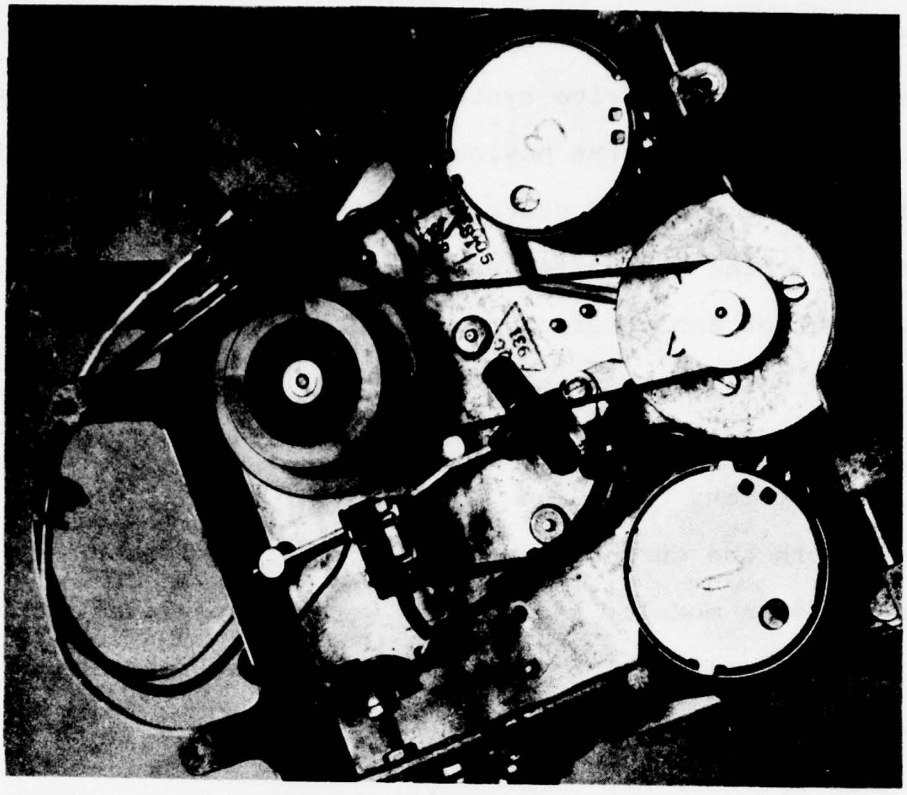


Figure 3. Underside of the tape deck showing inadequate rubber belt used to drive the capstan.

C. Excessive end play in the capstan shaft had to be reduced.

D. An amplifier with bias circuitry for recording was built.

During a test in March 1977, it was found that a 1 KHz signal recorded on the tape during vibration could not be recovered as a useable signal; there was too much distortion. It was decided to modify the belt drive system (Figure 3) to reduce speed changes due to belt movement. The modifications of the belt drive were put off to a future date. It was decided to use T/M to send the signals back, rather than record them for future retrieval.

3.4 Schedule Considerations

At this time, due to the pressure of the A24.609-1 launch schedule, it was decided to forego temporarily further development of the tape drive system; that portion of the system was to be replaced by the payload's FM/FM TM system, relaying data directly to a ground station. Efforts were now concentrated on developing the buffer and compression amplifiers.

3.5 Buffer Amplifier

An amplifier for each transducer was designed and built using a 741 general purpose operational amplifier. The amplifier had a gain of ten.

Both the current source and buffer amplifier were mounted in the same module; these parts were encapsulated and tested with a typical calibration (see Figure 4). The response is flat from less than 100 Hz to 3,000 Hz.

3.6 Compressor Amp

If the first buffer amp has a gain of 10, then an initial gain of 10 in the compressor amp will bring the output up to 1,500 mv for a transducer output of 15 mv (and a buffer output of 150 mv).

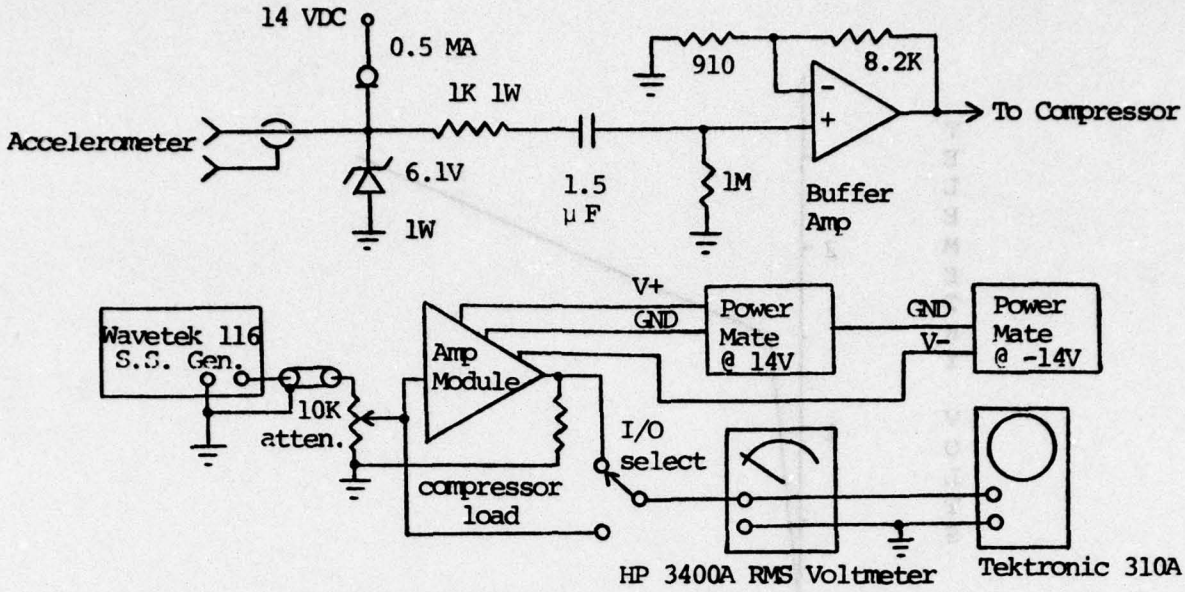
As the transducer goes from 15 mv to 200 mv, the buffer will output from 150 mv to 2,000 mv. For our purposes, it is desirable that the compressor go from 1,500 mv to 2,500 mv.

The compressor gain corner was set at 1.5v output, giving low level vibration the most sensitivity (see Figure 5a).

1 g/v expanded

18.5 g/v compressed

After these units were built (see Figure 5b), they were calibrated. (There is a difference between ideal diodes and the actual diodes used as noted on the transfer curve -- see Figure 5c.)



Output Voltage

f (Hz)	1mV	10mV	20mV	40mV	80mV	100mV
10	0.00560	0.04740	0.09500	0.1900	0.3750	0.4820
20	0.00720	0.07250	0.14500	0.2920	0.5840	0.7470
30	0.00930	0.08530	0.17200	0.3450	0.6880	0.8910
40	0.01000	0.09310	0.18700	0.3770	0.7500	0.9700
50	0.01030	0.09950	0.19500	0.3920	0.7840	1.0025
60	interference	0.10100	0.20200	0.4020	0.8070	1.0050
70	0.01070	0.10200	0.20400	0.4100	0.8250	1.0070
80	0.01080	0.102500	0.20730	0.4170	0.8320	1.0100
90	0.01085	0.103200	0.20810	0.4200	0.8400	1.0100
100	0.01125	0.104000	0.21000	0.4210	0.8420	1.0120
150	0.01160	0.105200	0.21400	0.4300	0.8597	1.0140
200	0.01160	0.105200	0.21400	0.43100	0.8620	1.0150
300	0.01160	0.105300	0.21600	0.43100	0.8698	1.0150
1K	0.01160	0.10700	0.21700	0.43500	0.8700	1.0160
3K	0.01160	0.10700	0.21700	0.43500	0.8700	1.0160

Figure 4. Calibration set-up of the Buffer Amplifier

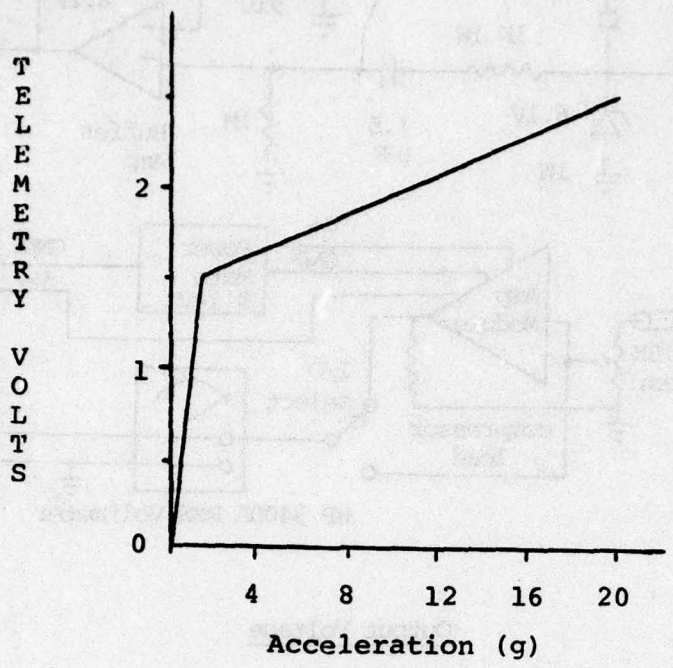


Figure 5a. Compressor and Expander Response

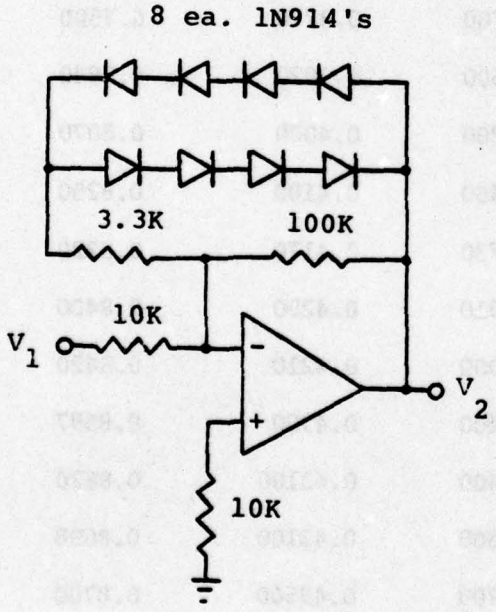


Figure 5b. Compressor Schematic

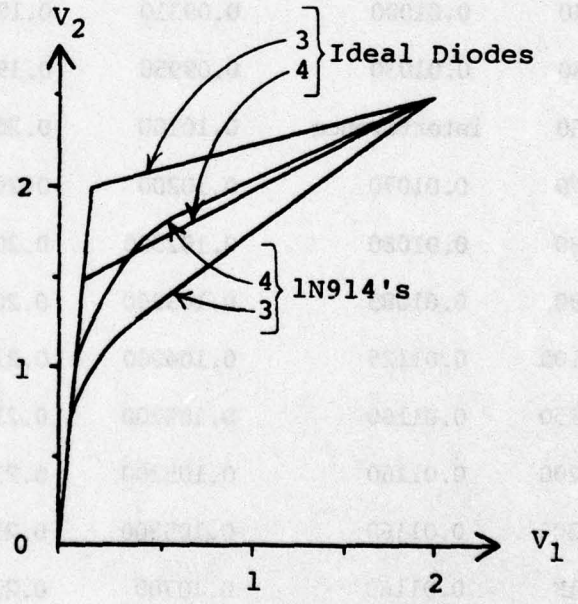


Figure 5c. Transfer Characteristics

The expander circuit was to be the inverse of the compressor; and again it would be checked, since there would be two critical points in compressor-expander compatability (see Figure 5a):

1. Low to high gain ratios must be the same.
2. Break points must come at the same T/M, input and output voltage.

These calibration tests were performed as in Figure 6 with typical results indicated. To insure compatability with T/M standards, a clamp circuit was added to ensure that shock or vibration levels in excess of the required 20 "G" maximum would be limited to ± 3.0v.

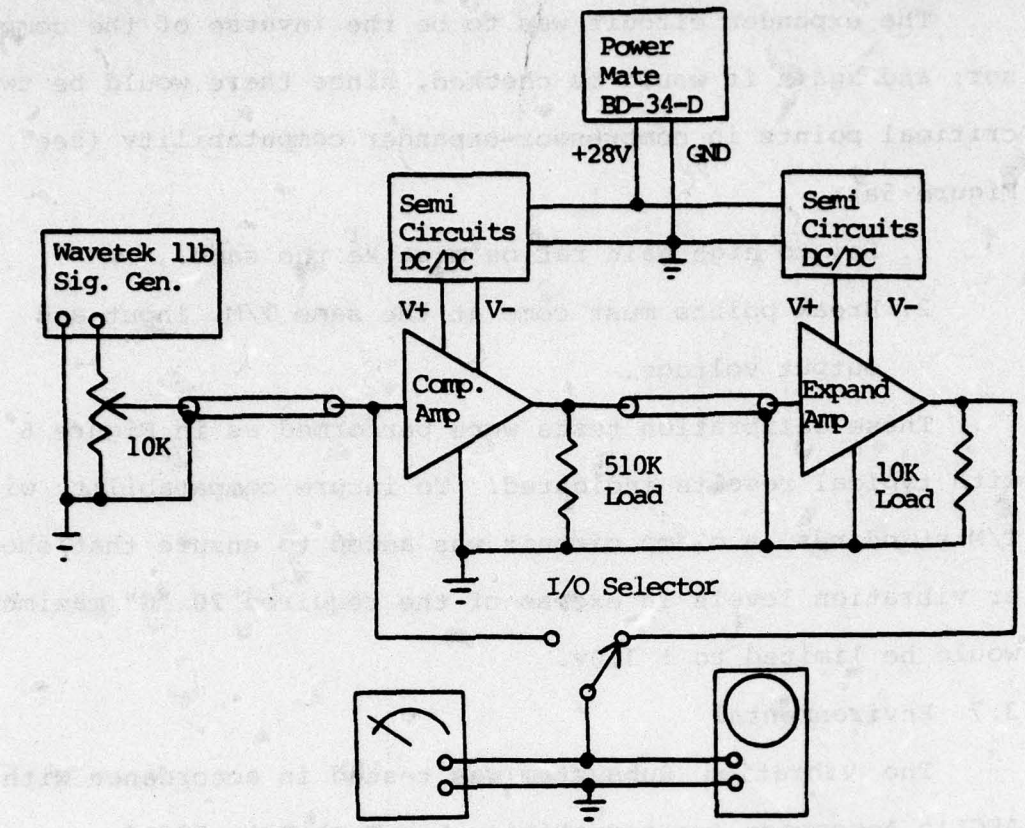
3.7 Environmental

The Vibration Subsystem was tested in accordance with AFGL's Aerospace Instrumentation Lab Tech Data #76-4.

4.0 SYSTEM CALIBRATION

System calibration was begun in June 1977 (see Figure 7). It was done by using the vibration facilities at AFGL to excite the BBN transducer and by using the analysis portion of the TDV53PSS (Time Data Vibration/Shock Control and Analysis Computer System).

The system is used to program and control the frequency, G level and duration of either vibration or shock tests. The signal from a control accelerometer mounted on the shaker table is compared with the programmed signal. The difference between them is used to automatically adjust the shaker table operation so that it conforms to the test program values.



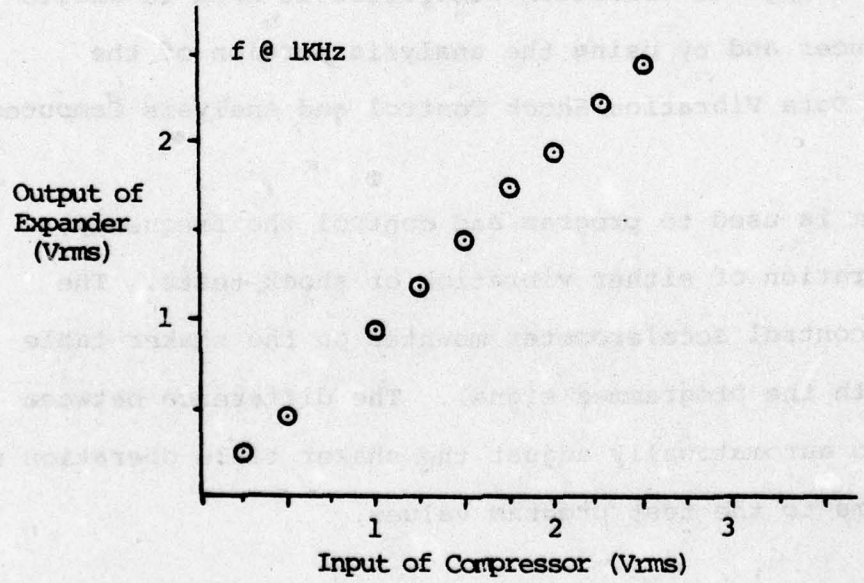
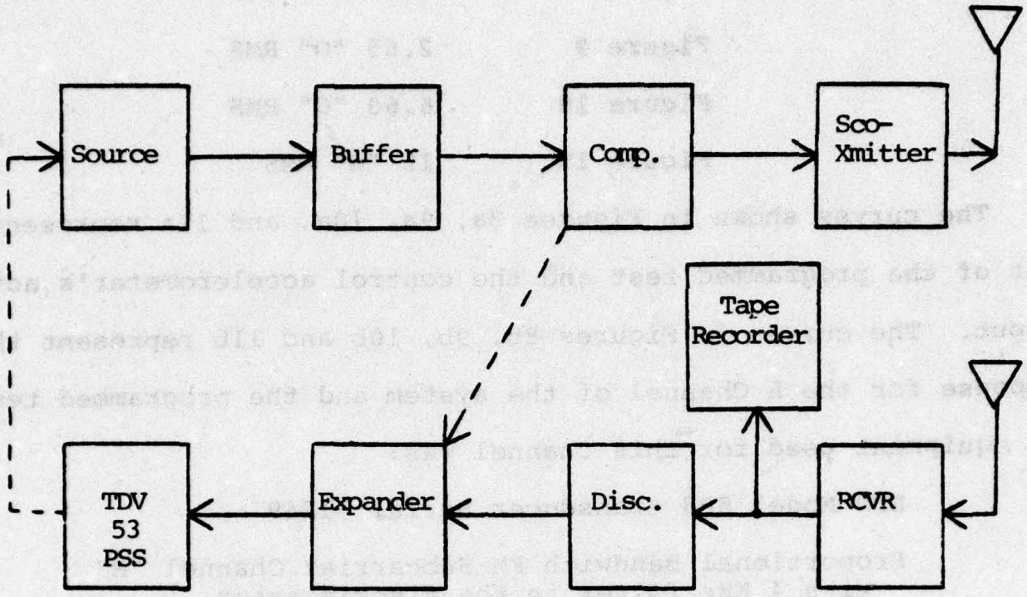


Figure 6. The test set-up for calibrating expander and compressor



Source

TDV 53 PSS

Wavetek 132 Noise Gen.
BBN 508/Vib transducer

Figure 7. Calibration set-up
for ROVIR system

The TDV53PSS was first used to compare the signal from the ROVIR to a signal from the Wavetek Model 132 Noise Generator. With this set, each channel of the system was checked and the outputs from each expander were adjusted.

After the adjustments were made, the telemetry system (see Figure 7) was added; this introduced new problems to the calibrating progress. The output from the discriminators had to be accurately set to obtain results similar to the first checks; the difference between two of the section's calibrators caused many problems.

The following curves were obtained when the BBN transducers were put into the system and driven by the shaker table:

Figure 8	.27 "G" RMS
Figure 9	2.65 "G" RMS
Figure 10	6.60 "G" RMS
Figure 11	15 "G" RMS

The curves shown in Figures 8a, 9a, 10a, and 11a represent a plot of the programmed test and the control accelerometer's actual output. The curves in Figures 8b, 9b, 10b and 11b represent the response for the A Channel of the system and the programmed test. The equipment used for this channel was:

BBN Model 508 transducer Serial #1249

Proportional Bandwith FM Subcarrier Channel "H" with 4 KHz filter in the discriminator.

Potted Module #1

Expander A

The curves shown in Figures 8c, 9c, 10c and 11c represent the response for the B Channel of the system and the programmed test. The equipment used for this channel was:

BBN Model 508 transducer Serial #1099

Proportional Bandwith FM Subcarrier Channel "F" with 3 KHz filter in the discriminator.

Potted Module #0

Expander B

The curves shown in Figures 8d, 9d, 10d and 11d represent the response for the C channel of the system and the programmed test. The equipment used for this channel was:

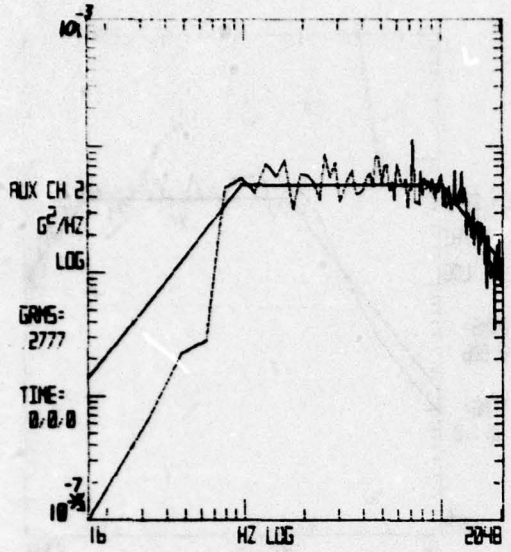


Figure 8a

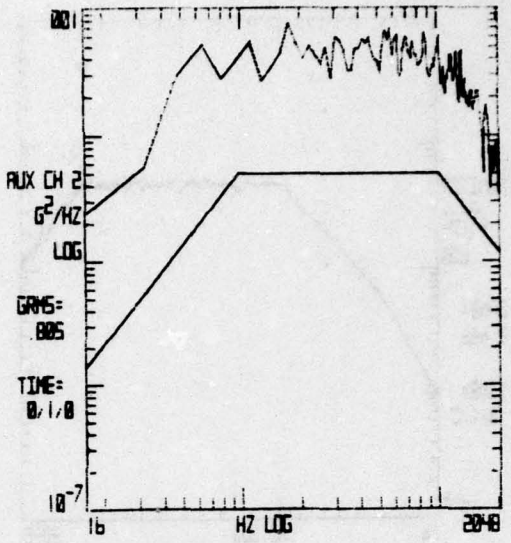


Figure 8b

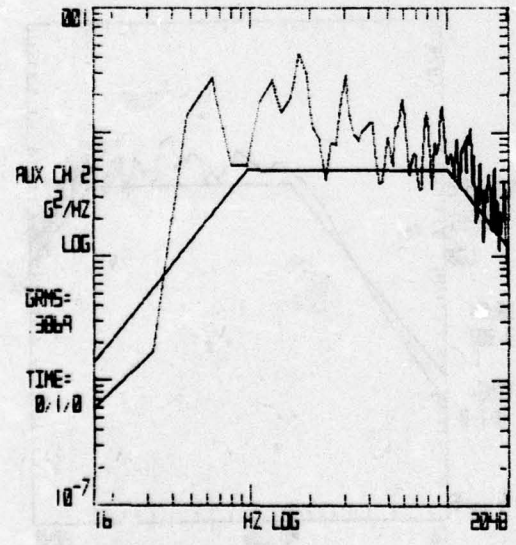


Figure 8c

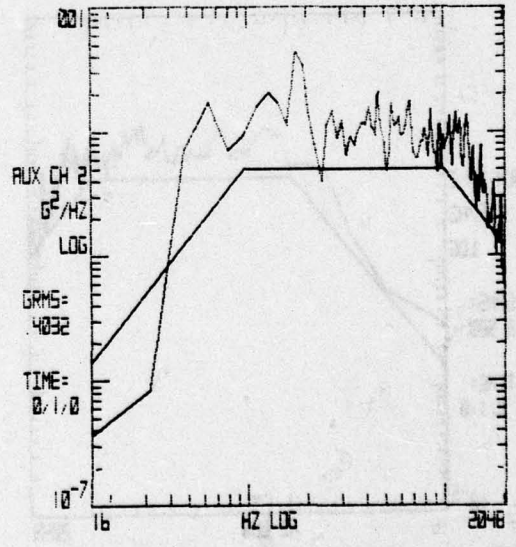
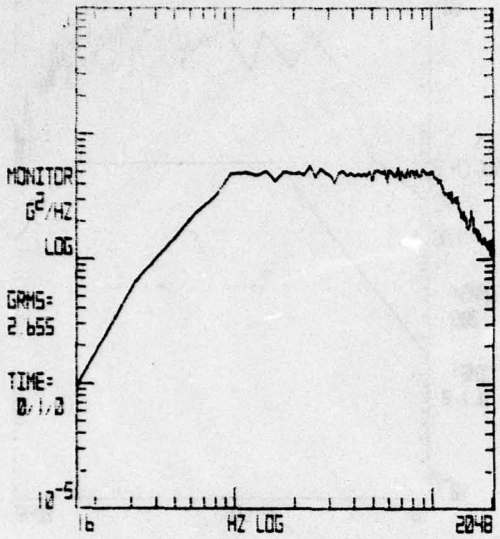


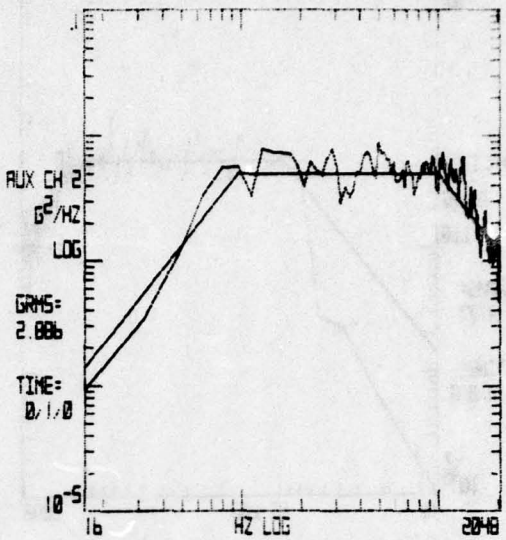
Figure 8d

Figure 8. .27 "G" RMS Calibration



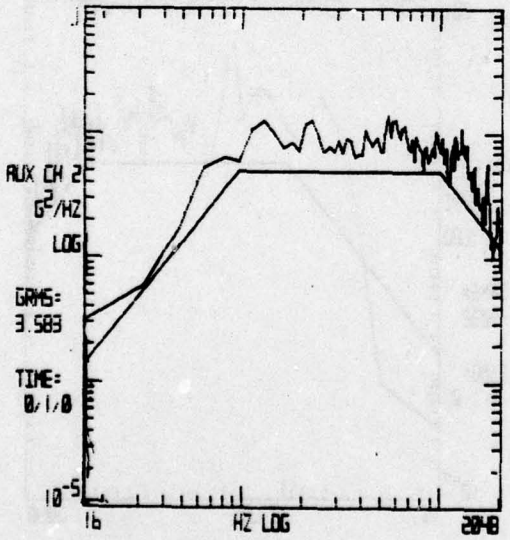
RANDOM ANALYSIS X AXIS 29 JULY 77
ROVIR SHAKE DIRECT

Figure 9a



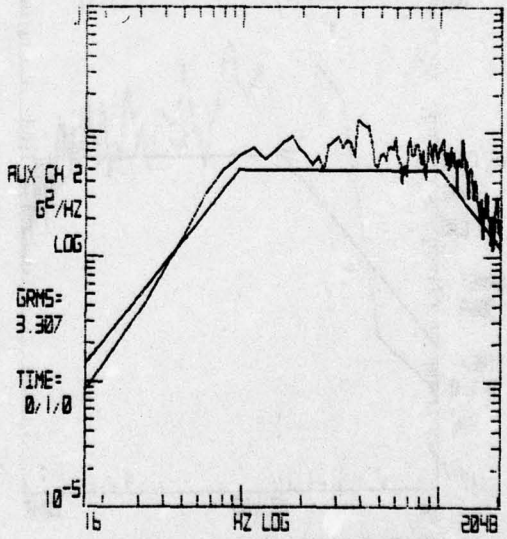
RANDOM ANALYSIS X AXIS 29 JULY 77
ROVIR SHAKE W/A EXP

Figure 9b



RANDOM ANALYSIS X AXIS 29 JULY 77
ROVIR SHAKE W/B EXP

Figure 9c



RANDOM ANALYSIS X AXIS 29 JULY 77
ROVIR SHAKE W/C EXP

Figure 9d

Figure 9. 2.65 "G" RMS Calibration

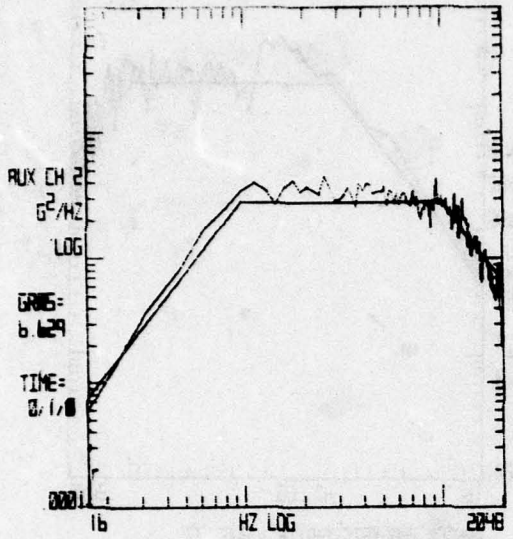


Figure 10a

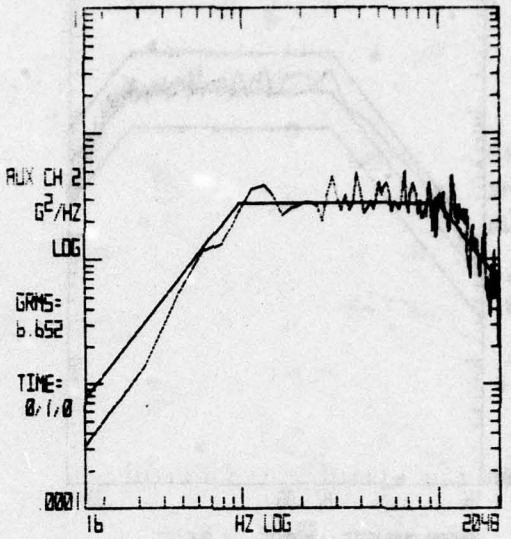


Figure 10b

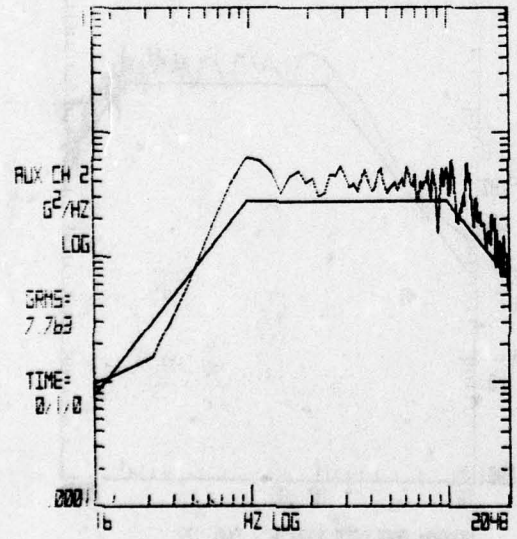


Figure 10c

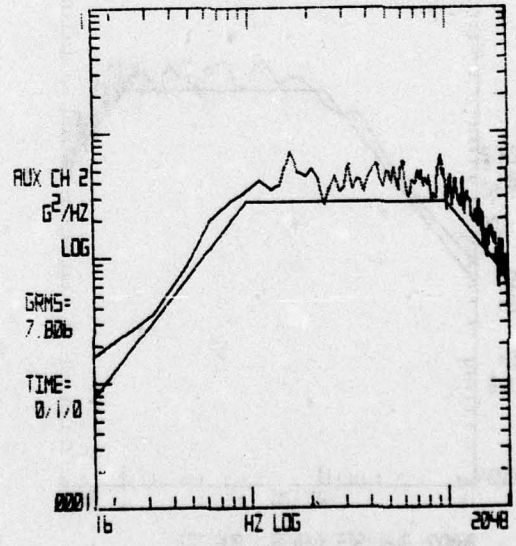
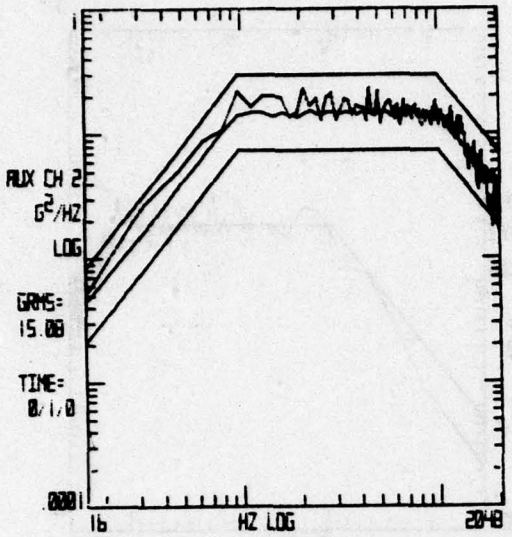


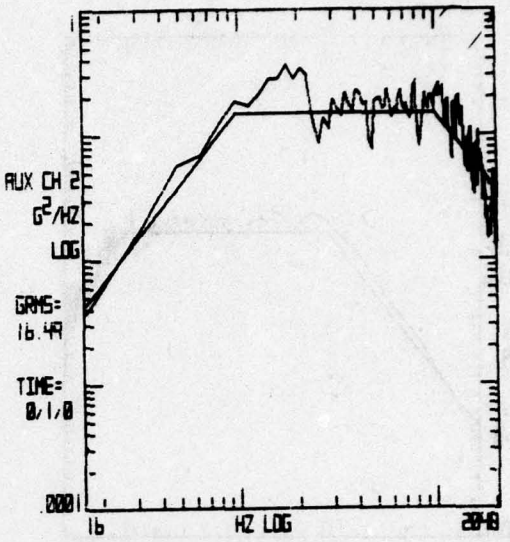
Figure 10d

Figure 10. 6.60 "G" RMS Calibration



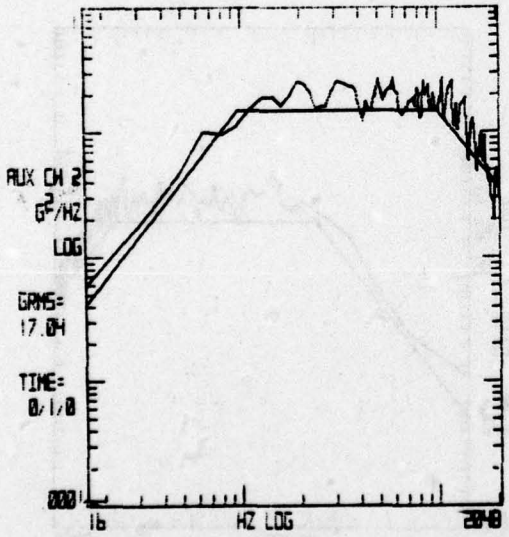
RANDOM ANALYSIS X-AXIS | AUG 77
ROVIR SHAKE W/C DIRECT

Figure 11a



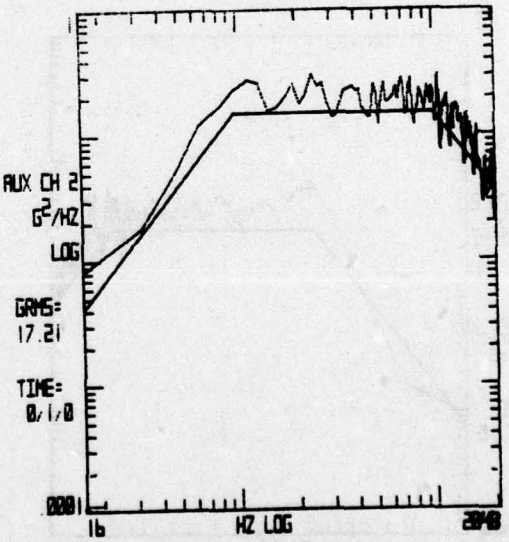
RANDOM ANALYSIS X-AXIS | AUG. 77
ROVIR TM W/A EXP.

Figure 11b



RANDOM ANALYSIS X-AXIS | AUG. 77
ROVIR TM W/B EXP.

Figure 11c



RANDOM ANALYSIS X-AXIS | AUG. 77
ROVIR TM W/C EXP.

Figure 11d

Figure 11. 15 "G" RMS Calibration

BBN Model 508 transducer Serial #1263

Proportional Bandwith FM Subcarrier Channel "D"
with 3 KHz filter in the discriminator.

Potted Module #3

Expander C

4.1 Shock Calibration

The shock calibration for the system was done at two different levels. The Time Data Shock synthesis system with TFE option program was used to drive the shaker table. Data from the shocked transducers was recorded on magnetic tape and reduced, using the Time Data Transient Waveform Control System program.

First shock was 1/2 level of	+23.51	-22.37 G'
TM Record/Processed "D"	+17.89	-12.91
TM Record/Processed "F"	+18.99	-14.74
TM Record/Processed "H"	+11.12	-14.74
Second shock was the full level of	+47.02	-44.74
TM Record/Processed "D"	+34.59	-26.73
TM Record/Processed "F"	+33.06	-29.39
TM Record/Processed "H"	+23.48	-27.60

The resulting 1/2 level shock is shown in Figure 12a; spectral response is indicated in Figure 13. The resulting full level shock is shown in Figure 14; its spectral response is indicated in Figure 15.

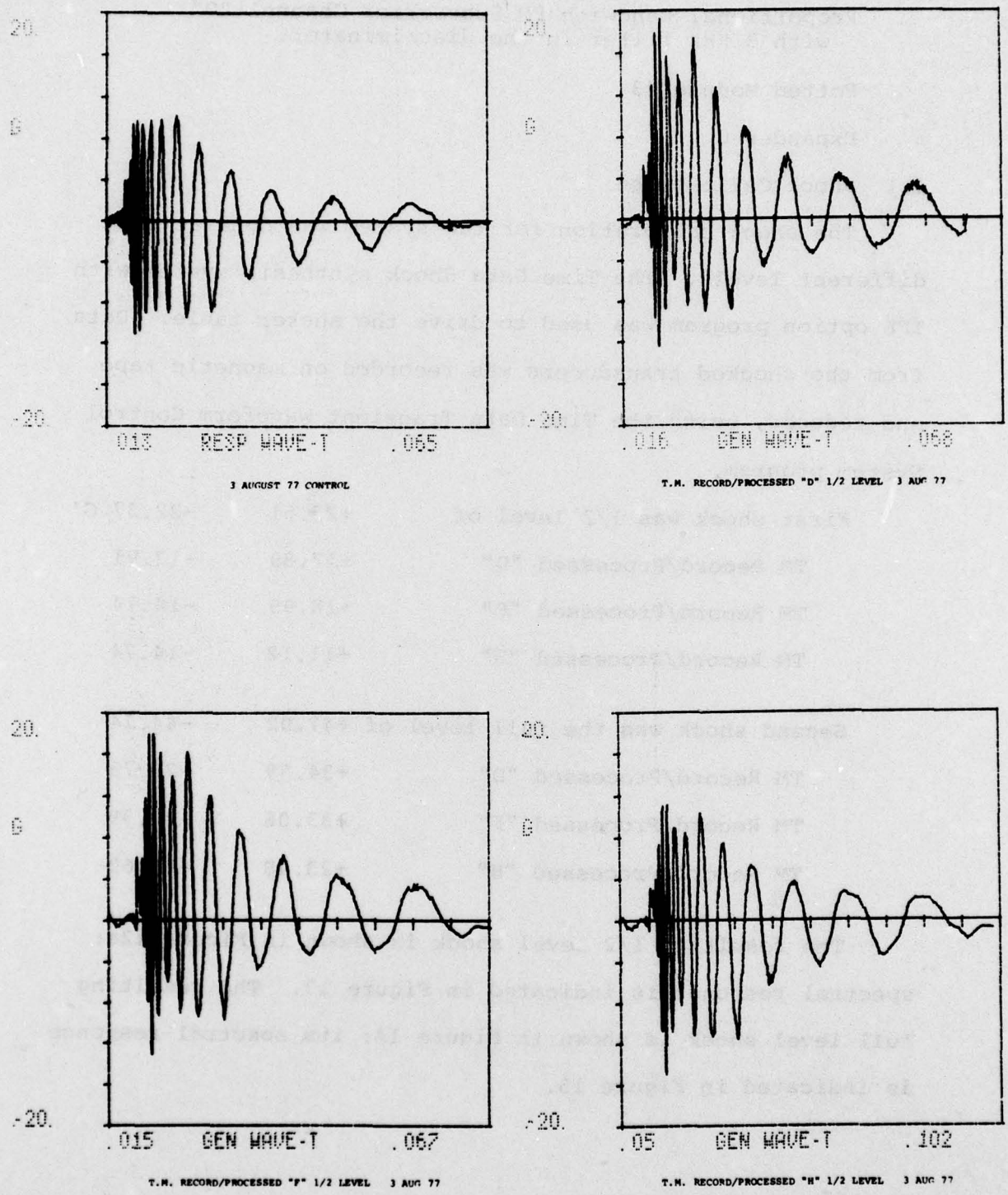
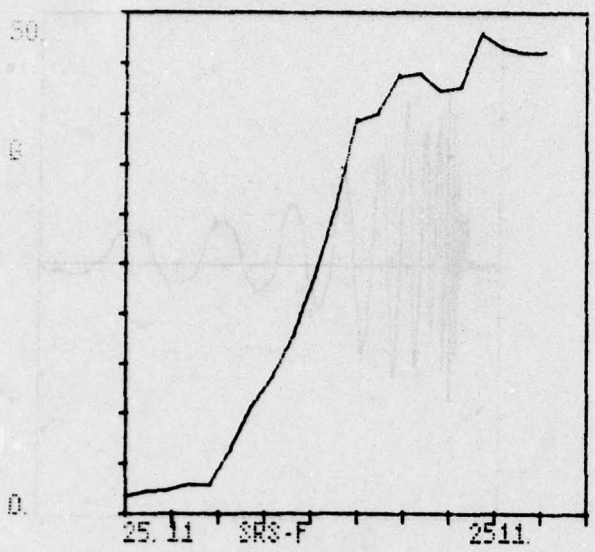
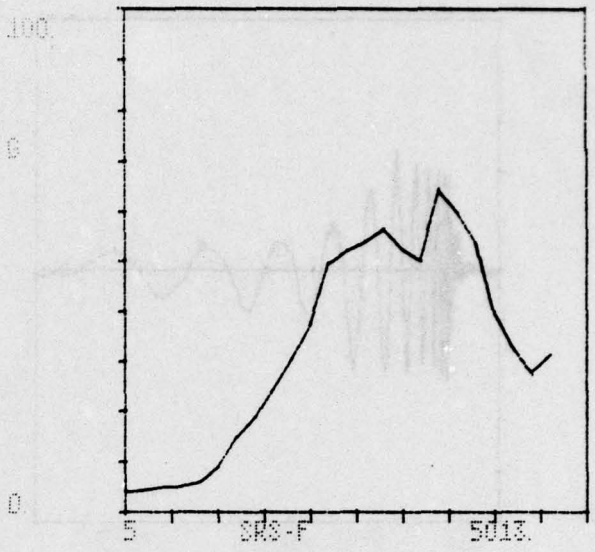


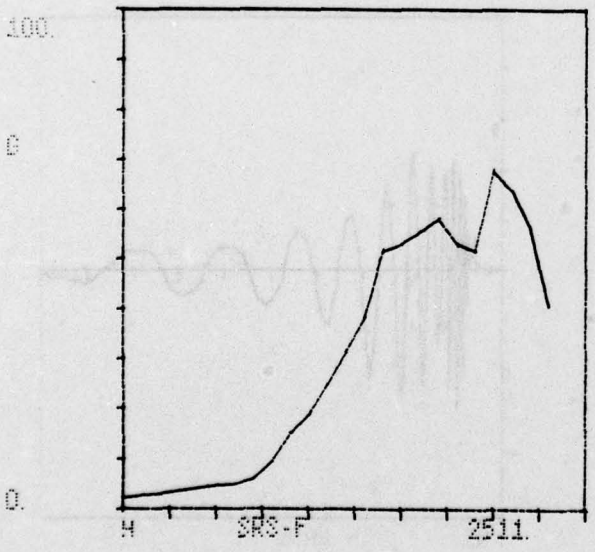
Figure 12. Half-Level Shock Test



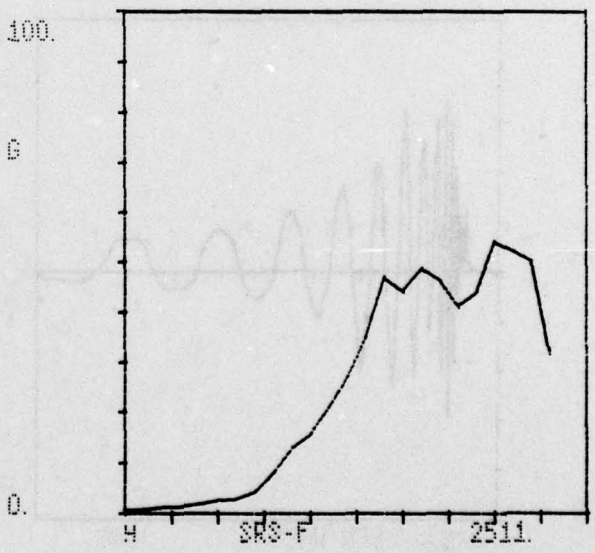
3 AUGUST 77 CONTROL 1



T.M. RECORD/PROCESSED "D" 1/2 LEVEL 3 AUG 77

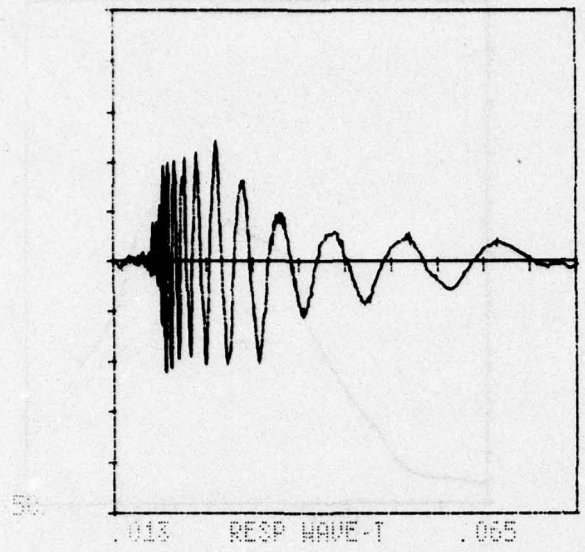


T.M. RECORD/PROCESSED "F" 1/2 LEVEL 3 AUG 77

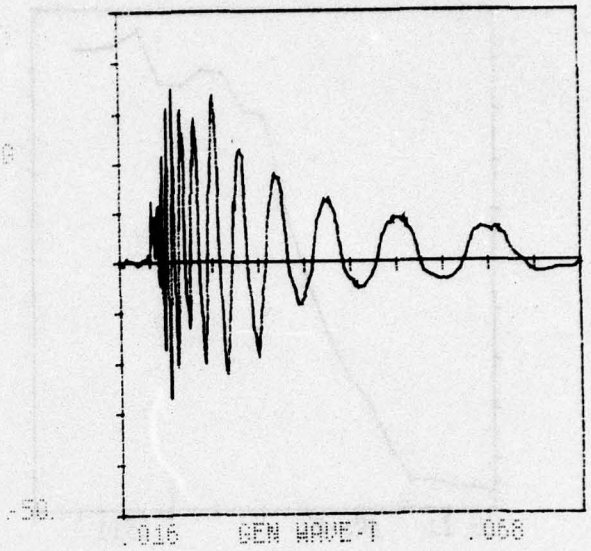


T.M. RECORD/PROCESSED "H" 1/2 LEVEL 3 AUG 77

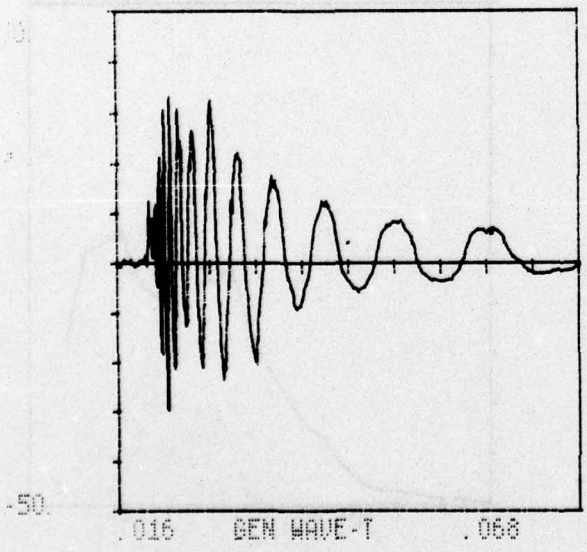
Figure 13. Spectral Response for Half-Level Shock



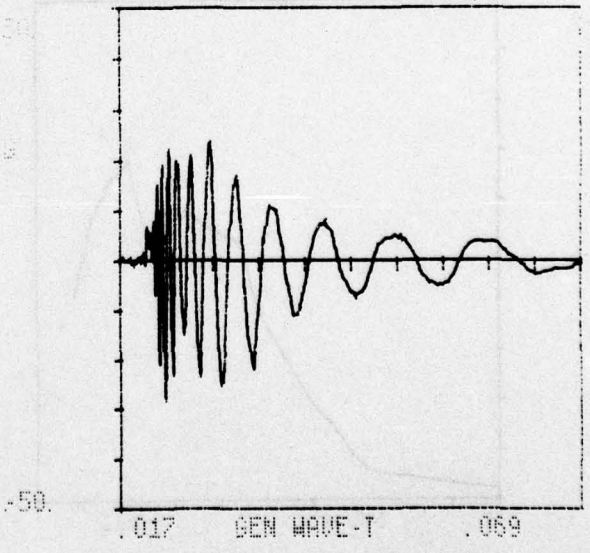
3 AUGUST 77 CONTROL



T.M. RECORD/PROCESSED "D" FULL LEVEL 3 AUG 77



T.M. RECORD/PROCESSED "F" FULL LEVEL 3 AUG 77



T.M. RECORD/PROCESSED "H" FULL LEVEL 3 AUG 77

Figure 14. Full Level Shock Test

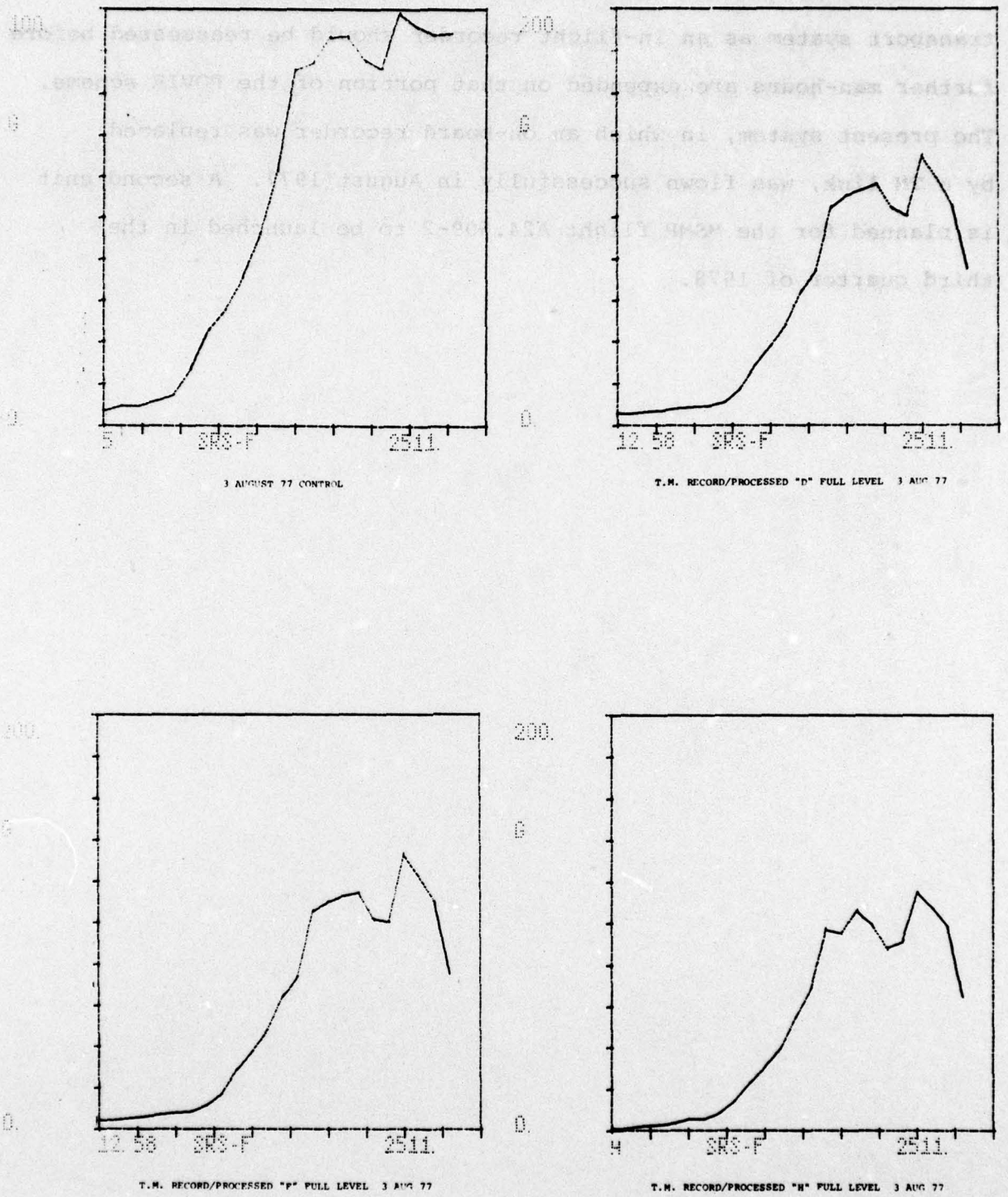


Figure 15. Spectral Response for Full Level Shock

5.0 CONCLUSION

The likelihood of successfully using an inexpensive tape transport system as an in-flight recorder should be reassessed before further man-hours are expended on that portion of the ROVIR scheme. The present system, in which an on-board recorder was replaced by a TM link, was flown successfully in August 1977. A second unit is planned for the MSMP flight A24.609-2 to be launched in the third quarter of 1978.

C.D.S.F.U. Function Monitor Update

1.0 INTRODUCTION

An earlier Scientific Report (Green, Owen R., Wentworth Institute of Technology, Boston, Mass.; "A Capacitor Discharge Squib Firing Unit", AFCRL-TR-75-0620, 1 April 1975) described the development of a system for igniting EEDs (Electroexplosive Devices). This system used the energy stored in a bank of capacitors to ignite as many as four of the standard bridge wires simultaneously. (A standard bridge has 1 ohm resistance). This system, known as the C.D.S.F.U. (Capacitor Discharge Squib Firing Unit) employs two forms of function monitoring. At the time the report was prepared, in-flight data was available to illustrate only one of these forms -- the one that monitored current flow of the discharge. Since then, data has become available which illustrates an alternate monitoring method. This report section updates the original report by demonstrating the usefulness of this second method.

2.0 RELATIVE MERITS

The alternate method of monitoring measures the voltage across the capacitor bank. The major difference between the two monitoring methods is the length of the output signal. The current monitor signal is rather short, approximately 0.1 ms to 0.5 ms long. It requires that T/M (Telemetry) have the ability to handle signals of 50KHz or more. The voltage monitor signal, approximately 0.01 sec to 0.5 sec long, can be monitored by T/M on 50Hz to 100Hz channels. This reduced T/M requirement may play an important part in deciding which method to use.

3.0 FLIGHT DATA

The C.D.S.F.U. firing data was obtained from the A31.604 flight carrying two units. Figure 1 shows graphs of this data. Each curve represents the instantaneous voltage across the capacitor bank; each shows the amount of discharge and the recharge rate. Table 1 summarizes the technical information relating to the graphs.

By examining the graphs, some comparison can be made between the number of squibs fired, the types of squibs fired, and the power supplied to these squibs by the C.D.S.F.U.

Note Curves 1a and 2a. These two curves show similar depths of discharge and overall power consumed. In both cases, two bellows and thrusters were fired simultaneously. Curve 3a is similar in shape, but it does not show as deep a discharge. In this case, only two thrusters were fired. Table 1 shows that curve 3a and 3b are both firing the same type of load -- two thrusters -- but notice that curve 3b used about half the power of curve 3a.

Footnote 2 in Table 1 indicates that in the case of curve 3b, the thruster had no mechanical load. The thruster of curve 3a had already released the mechanism before the thruster of curve 3b was ignited. It is suspected that without a mechanical load, the pressure and temperature inside this EED was different from its duplicate 3a; and that this difference reduced the current flow through the device. Current continues to flow intermittently through EEDs during the burning process. The amount of current flow appears to depend upon the burning process characteristics.

Table 1. Technical data for the graphs in Figure 1

Graph Number	Number of Bridgewires	Type of Squib	Number of Squibs
(1a)	4	Holex Thrusters Model #2900 with Insert #2118	2
		Hercules Bellows #BA60E1	2
(1b)	2	Holex Thrusters Model #2900 with Insert #2118	2
(2a)	4	Holex Guillotine Cutters Model #5800	2
		Hercules Bellows #BA60E1	2
(2b)	2	Holex Guillotine Cutters Model #5800	2
(3a)	4	Holex Thrusters Model #2900 with Insert #2118	2
(3b)	4	Holex Thrusters Model #2900 with Insert #2118	2
(4a)	1	SDI Inc. Miniature Thruster #103233	1
(4b)	1	SDI Inc. Miniature Thruster #103233	1

Footnote 1. Curves 1b and 2b are the result of the auxiliary C.D.S.F.U. attempting to ignite an EED that has already been fired by the primary C.D.S.F.U.

Footnote 2. Curve 3b is different from Curve 3a, even though both EEDs are similar, due to the fact that the thruster of 3b had no mechanical load. The device had been previously actuated by the thruster of Curve 3a.

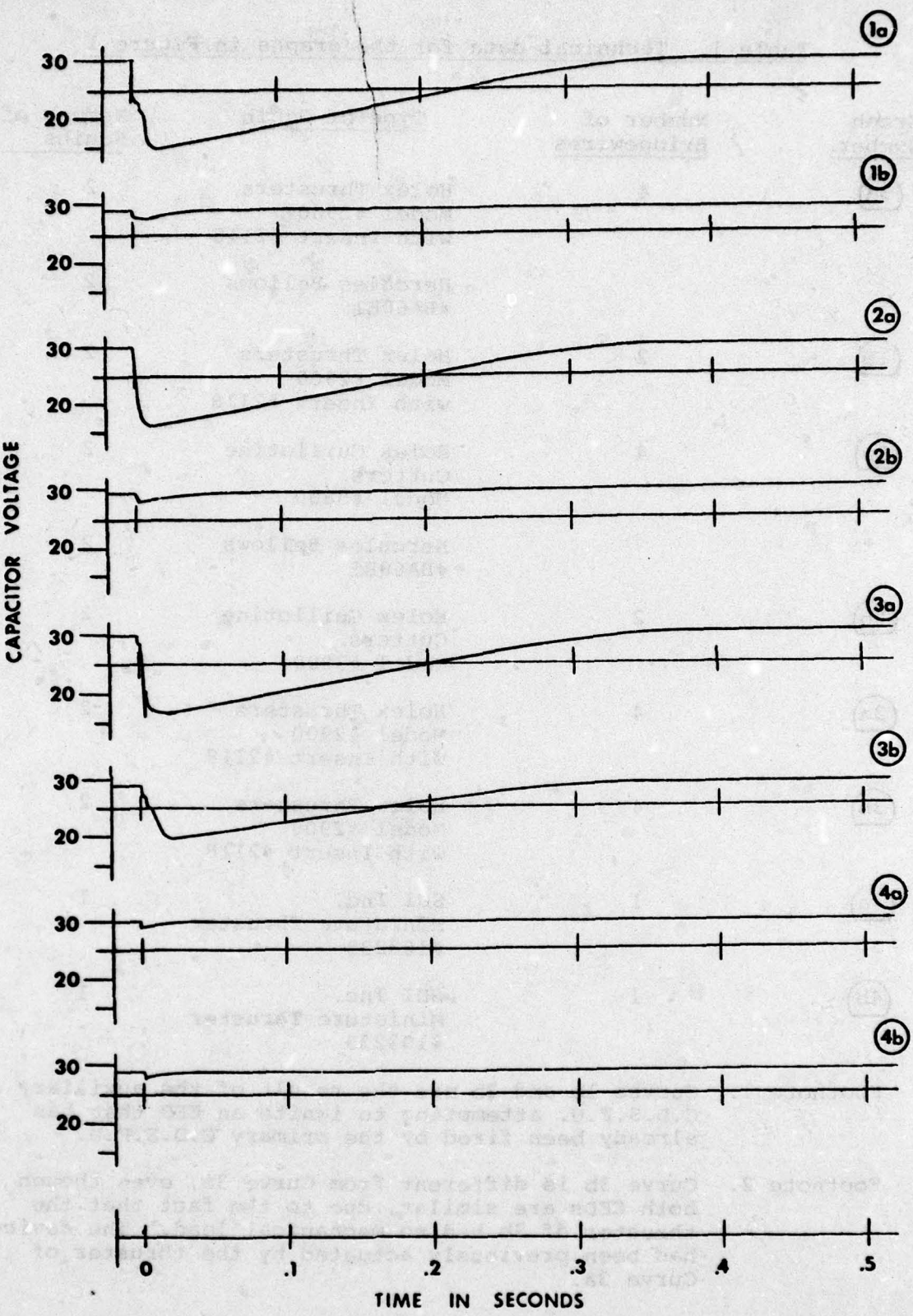


Figure 1. CAPACITOR VOLTAGE FOR EIGHT CD FIRINGS IN SOUNDING ROCKETS

Curves 1b, 2b, 4a and 4b are all similar in that they show a low level of power consumed when ignited. Curves 1b and 2b are the result of burning a second bridge wire in an EED that has already been fired by the first bridge. It is likely that a metal wire stripped of its primer is all that is left of these second bridges. Curves 1b and 2b show how little energy it takes to burn them through.

Curves 4a and 4b also show that a minimum amount of energy was used to ignite the S.D.I. INC miniature thrusters. Apparently, no electrical conduction takes place once the bridge wire burns through on this particular model squib.

4.0 CONCLUSION

Unlike the current monitor, the voltage monitor does not show the instantaneous power supplied to the squib; it does show the amount of power used and the amount of power still remaining in the capacitor bank. It also shows how long it takes to recharge the capacitor bank -- a feature not available when using only the current monitor system. In addition, the fact that the T/M requirements are less stringent for the capacitor bank voltage monitors, one may decide that it is the form of function monitoring that best fits a particular application.

Printed by
United States Air Force
Hanscom AFB, Mass. 01731